4x5 Carrier Boards Overview

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Revision: 0.1
Date: 26-Sep-2014 10:35

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TE0701 Carrier Board for TE07xx

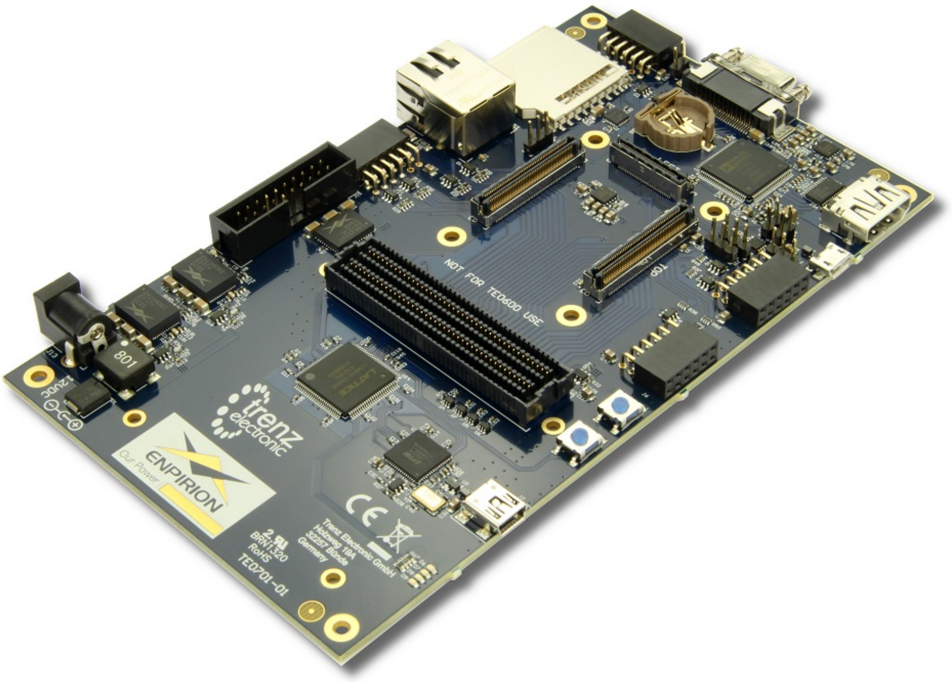


Figure 1: TE0701 (REV 01; only a limited number is released - a slightly modified REV 02 is shipped to customers).

TE0703 Carrier Board for TE07xx

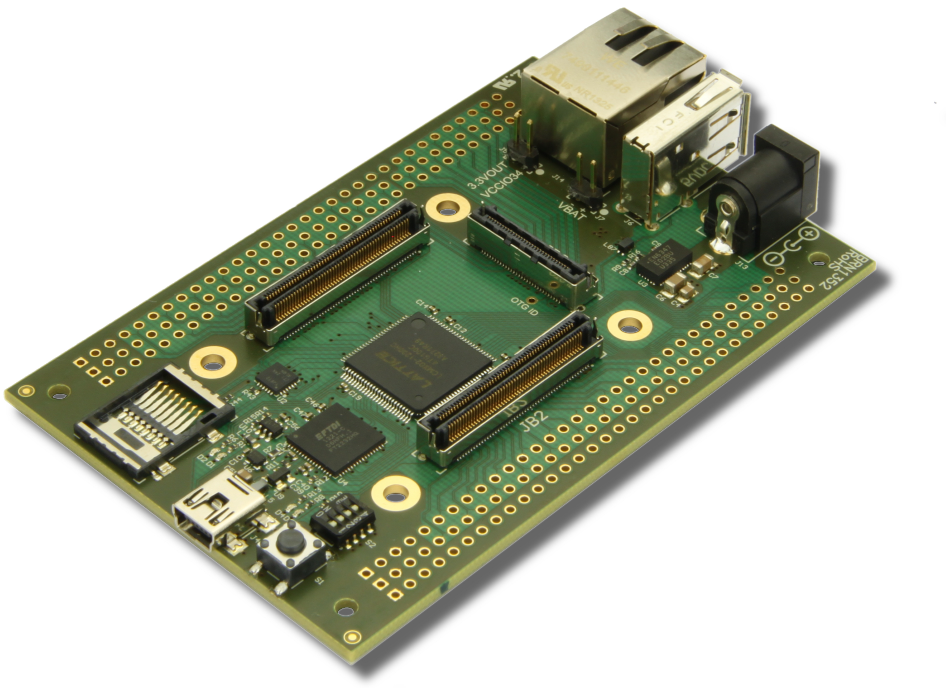


Figure 2: TE0703 (REV 01).

Document Change History

date	revision	authors	description
2014-01-05	0.1	Sven-Ole Voigt	Work in progress
	All	Sven-Ole Voigt	

TE0701 Carrier Board User Manual

Overview: TE0701 Carrier Board

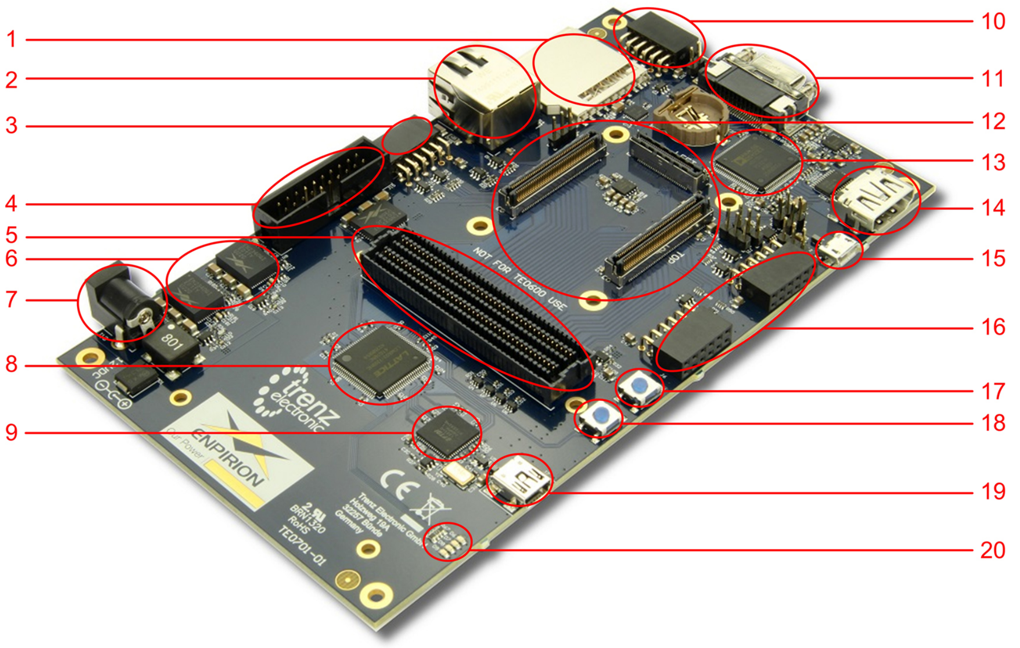


Figure 1a: TE0701-01 (REV 01; only a limited number is released - a slightly modificated REV 02 is shipped to customers).

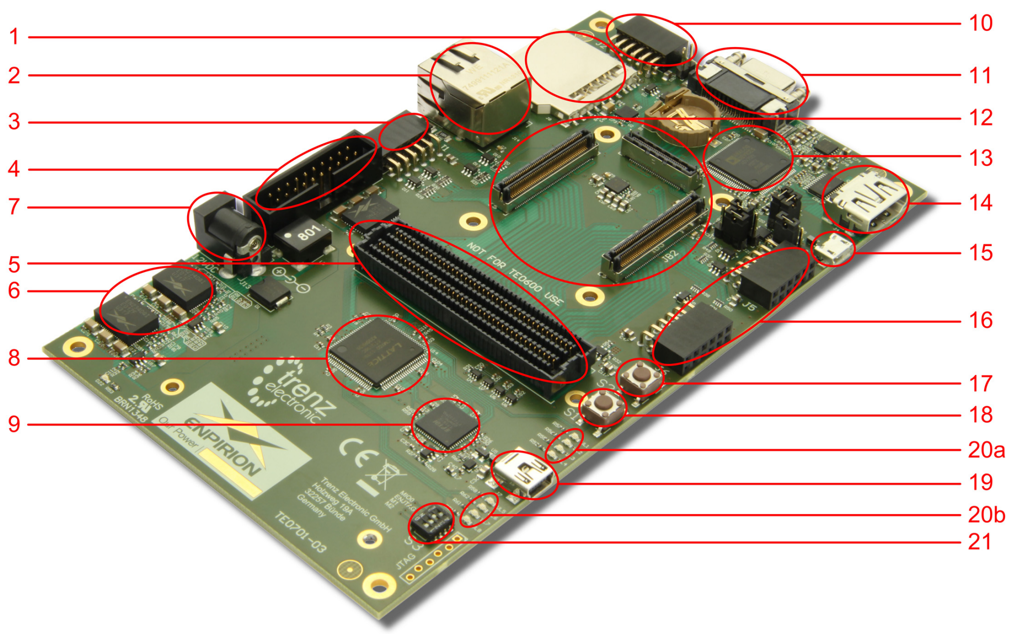


Figure 1b: TE0701-03 (REV 03).

Features

1. SD Card Connector - Zynq SDIO0 Bootable SD port (see TE0701 Carrier Board User Manual | Configuring Boot Mode)
2. RJ45 GbE Connector
3. Pmod Connector (J1, 3.3V): mapped to 8 Zynq PS MIO0 pins (MIO0, MIO9 to MIO15) when using TE0720 (same mapping as on Zedboard), 6 pins (MIO10 to MIO15) are additionally connected to TE0701 CPLD Carrier Controller
4. ARM JTAG Connector (DS-5 D-Stream, see TE0701 Carrier Board User Manual | ARM JTAG Bus) - PJTAG to EMIO multiplexing needed
5. VITA 57.1 compliant FMC LPC Connector with digitally programmable FMC VADJ Power Supply (see TE0701 Carrier Board User Manual | Configuring Power Supply)
6. High Performance Enpirion DC-DC Converters (EN2340QI) for 5.0V and 3.3V Power Supplies
7. Barrel jack for 12V Power Supply (**Note**: The local power supplies, 5.0V and 3.3V, are generated by high performance Enpirion DC-DC converters (EN2340QI) from the 12V power supply.)
8. Carrier Controller CPLD (Lattice LCMXO2-1200HC): 1,200 Macrocell CPLD with Block RAM, Flash and PLL;
   8 User LEDs and 2 User Pushbuttons mappable to different functions; VID and EN Control for FMC VADJ DC-DC Regulator (see TE0701 Carrier Board User Manual | Lattice CPLD Programming)
9. USB JTAG and UART Interface (FTDI FT2232H), compatible with Xilinx Tools (also with many other tools):
   Channel A can toggle Zynq SoC Module (PS) Reset, Channel B can be used as USB UART (TE0701 CPLD can reroute RXD/TXD signals)
10. Pmod Connector (J2, 3.3V): 6 pins (PX0 to PX7) can be multiplexed by Texas Instruments TXS02612RTWR SDIO Port Expander to SD Card pins (MIO1 bank when using TE0720), 2 pins connected to TE0701 CPLD Carrier Controller (PX6 and PX7)
11. Mini CameraLink Connector
12. Trenz 4x5 Module Socket (3x Samtec LSHM Series Connectors)
13. ADV7511 HDMI Transmitter
14. HDMI Connector (1.4 HEAC Support)
15. Micro USB Connector (Device, Host or OTG Modes)
16. 2x Pmods for Zynq PL (4 differential FPGA I/O Pins each)
17. User Push Button S2 ("RESTART", see TE0701 Carrier Board User Manual | User Push Buttons (PBs) and LEDs)
18. User Push Button S1 ("RESET", see TE0701 Carrier Board User Manual | User Push Buttons (PBs) and LEDs)
19. Mini USB Connector (USB JTAG and UART Interface, see TE0701 Carrier Board User Manual | JTAG Programming Guide or TE0701 Carrier Board User Manual | Connecting FTDI USB-to-UART/FIFO Interface)
20. User LEDs (function mapping depends on TE0701 CPLD Carrier Controller, see TE0701 Carrier Board User Manual | User Push Buttons (PBs) and LEDs)
21. User 4-bit DIP Switch (TE0701-03 only; see TE0701 Carrier Board User Manual | User Push Buttons (PBs) and LEDs)

Document Change History

date	revision	authors	description
2014-02-18	0.2	Sven-Ole Voigt	TE0701-03 (REV3) updated
2014-01-05	0.1	Sven-Ole Voigt	Initial release
	All	Sven-Ole Voigt	

TE0701 Jumper Configurations

> Press "<Strg> + <Pos1>" to return back to this overview!

Jumper Configurations

On the TE0701 carrier board (REV2) different hardware/software configurations can be chosen by the following 8 (TE0701-03: 6) jumpers and 4-bit DIP switch (TE0701-03 only):

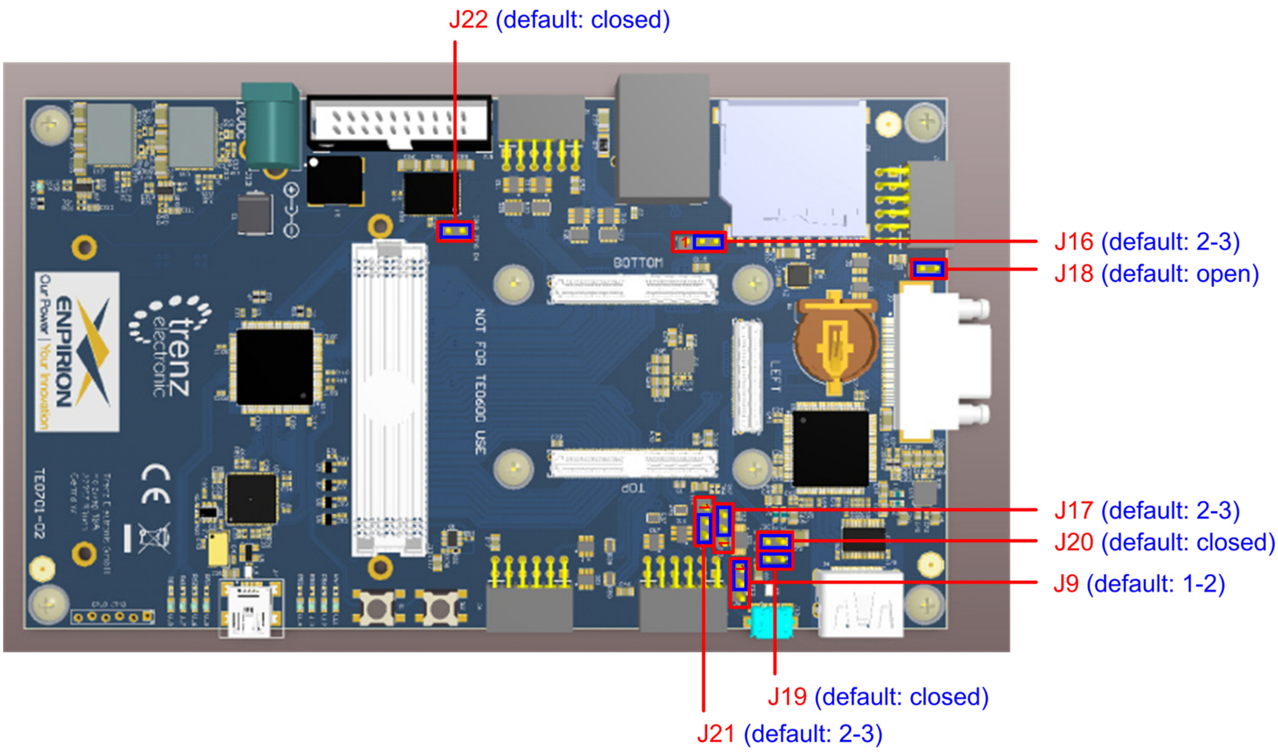


Figure 2a: TE0701-02 (REV2) Jumper Configurations.

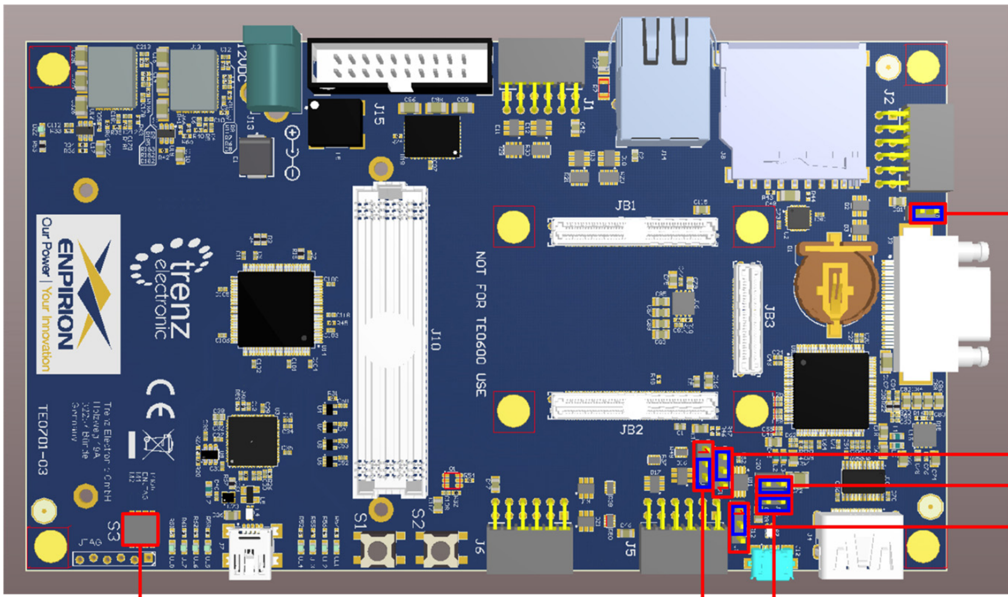


Figure 2b: TE0701-03 (REV3) Jumper Configurations.

Configuring Power Supply of the Micro USB Connector (Device, Host or OTG Modes)

The TE0701 carrier board can be configured as a USB host. Hence, it must provide from 5.25V to 4.75V to the board side of the downstream connection (micro USB port on J12; 13). To provide sufficient power, a TPS2051 power distribution switch is located on the carrier board in between the 5V power supply and the Vbus signal of the USB downstream port interface. If the output load exceeds the current-limit threshold, the TPS2051 limits the output current and pulls the overcurrent logic output (OC_n) low, which is routed to the on-board CPLD. The TPS2051 is put into operation by setting J19 CLOSED. J20 provides an extra 100µF decoupling capacitor (in addition to 10µF) to further stabilize the output signal. Moreover, a series terminating resistor of either 1K (J9: **1-2**, 3) or 10K (J9: 1, **2-3**) is selectable on the "USB-VBUS" signal. Both signals, USB-VBUS and VBUS_V_EN (that enables the TPS2051 on "high") are routed (as well as the corresponding D+/- data lines) via the on-board connector directly to the USB 2.0 high-speed transceiver PHY from SMSC (USB3320) on the GigaZee module, which is, in turn, connected to the Zynq FPGA. In summary, the default jumper settings are the following: J9: **1-2**, 3 (1K series terminating resistor); J19: CLOSED (TPS2051 in operation); J20: CLOSED (100 µF added).

> Additionally, the TE0701 carrier board is equipped with a second mini USB port (J7; see (19) in Figure 1 of TE0701 Carrier Board User Manual) that is connected to a "USB to multi-purpose UART/FIFO IC" from FTDI (FT2232HQ) and provides a USB-to-JTAG interface between a host PC and the TE0701 carrier board and the TE0720 Zynq module, respectively. Because it acts as a USB function device, no power switch is required (and only a ESD protection must be provided) in this case.

Configuring CPLD JTAG Mode

The JTAG port of the CPLD is enabled by setting J22 on TE0701-02 (REV2) or by setting DIP switch S3 on TE0701-03 (REV3):

- TE0701-02 (REV2): Jumper J22 labeled "CPLD JTAG EN" (see Figure 2) has to be REMOVED to enable CPLD JTAG mode, because only if the corresponding CPLD input pin JTAGENB is configured "high", the I/O pins TDI, TDO, TMS, and TCK will function as JTAG pins (see Lattice DS135, p.4-1). **Note**: Setting J22 CLOSED will tie JTAGENB to ground, i.e., TDI, TDO, TMS, and TCK will function as general purpose I/O pins!
- TE0701-03 (REV3): DIP switch S3 labeled "ENJTAG" must be moved to OFF position.

Configuring Power Supply of the TE0720 Zynq SoC Module

The TE7020-GigaZee board can be powered either by 3.3V (J16: **1-2**, 3) or 5.0V (J16: 1, **2-3**). The latter is the default setting (i.e., VIN=5.0V) to maximize the power that can be provided to the TE0720-Gigazee board considering the maximum current of 2A per pin on the board-to-board SAMTEC LSHM Series Connector.

J16 is not available on the TE0720-03 (REV3) Carrier Board anymore! Instead the modules' power supply is now fixed to 5V power supply!

Additionally, the VCCIO33 and VCCIO34 supply voltages of the Zynq FPGA (on bank 33 and bank 34, respectively) can be selected either to be 3.3V (J17: **1-2**, 3) or 2.5V (J17: 1, **2-3**). The latter is the default setting (i.e., VCCIO33=VCCIO34=2.5V). Furthermore, the VCCIO13 supply voltage (bank 13) can be selected to be either identical to bank 33/34 (J21: **1-2**, 3) or to be FMC_VADJ (J21: 1, **2-3**). Again, the latter is the default setting (i.e., VCCIO13=FMC_VADJ). **Note**: The differential signals FMC_LA17 to FMC_LA33 (next to PB0 to PB3 as well as Y0 to Y5) are routed to bank 13 of the Zynq FPGA, hence, the VCCIO13 supply voltage is chosen correspondingly by default!

The FMC power supply on the TE0701 Carrier Board (i.e., FMC_VADJ) is user programmable via I2C. Please consult Carrier Boards for TE0720 | Configuring FMC Power Supply Voltage on TE0701 via I2C for more details!

Configuring 12V Power Supply Pin on the Camera Link Connector

Finally, a 12V power supply can be connected to pin 26 of the camera link by closing J18. However, this option is disabled by default (J18: OPEN).

TE0701 JTAG Programming Guide

Press "<Strg> + <Pos1>" to return back to this overview!

JTAG Programming Guide

The Lattice CPLD on TE0701 carrier board as well as the Xilinx Zynq FPGA on the TE0720-GigaZee board can be programmed via JTAG. In the following figures the dedicated JTAG chains are illustrated:

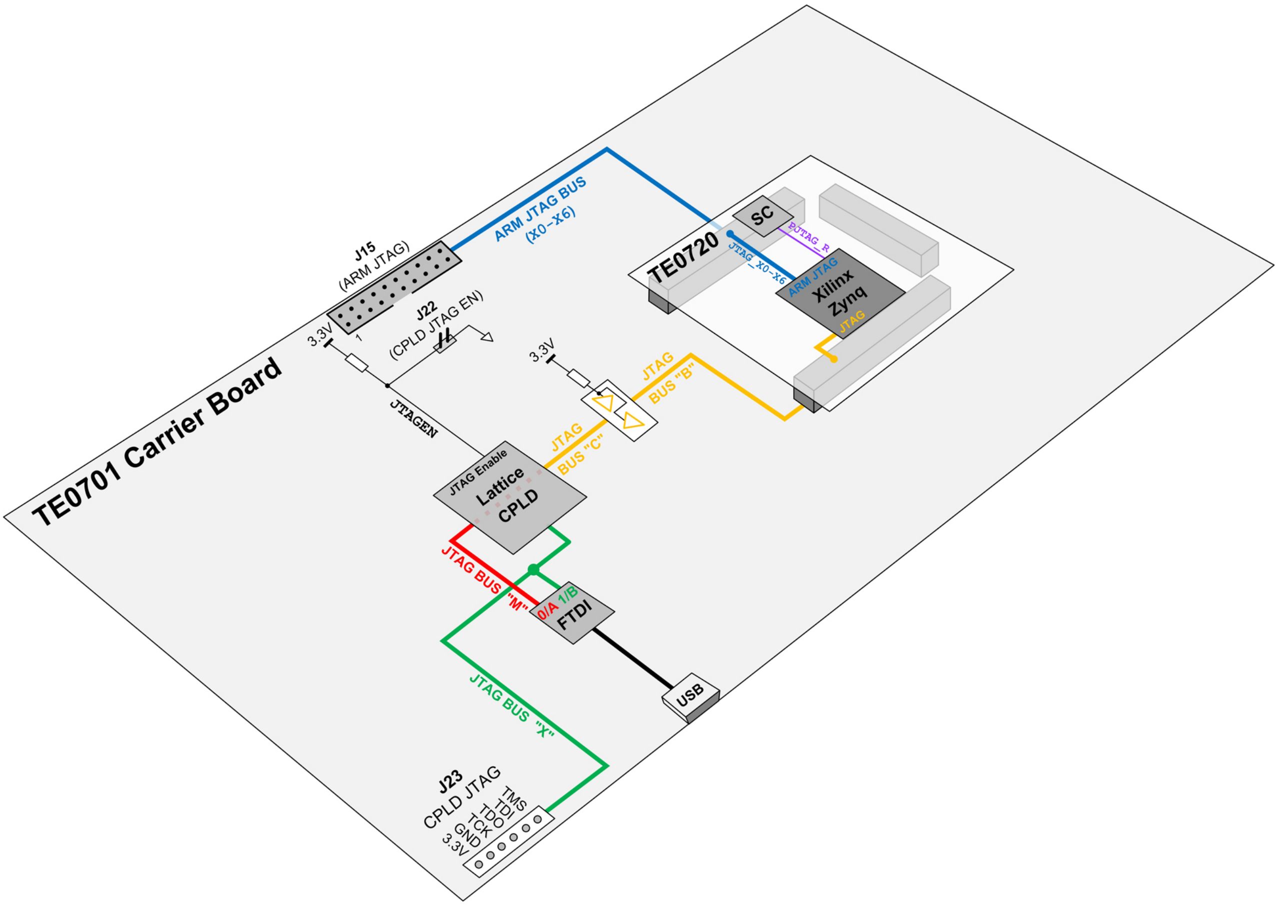


Figure 3a: TE0701 (REV2) and TE0720 (REV1) JTAG Chains.

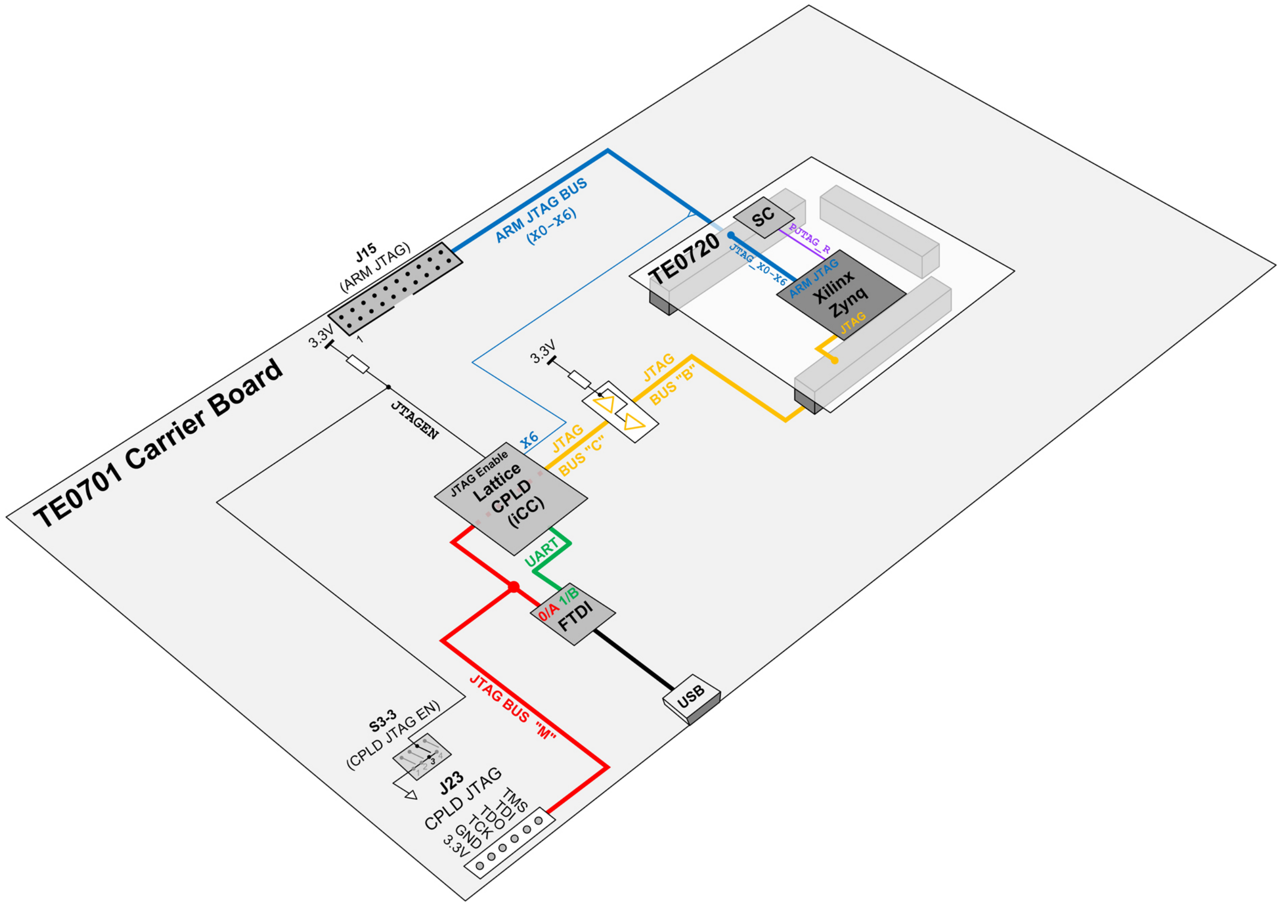


Figure 3b: TE0701 (REV3) JTAG Chains.

As it can be seen, the most convenient way to configure both devices mentioned above will be via the FTDI USB-to-JTAG interface that is supported by both the *Lattice Diamond Design Software* and the *Xilinx ISE Design Suite* as described in the following sections:

Lattice CPLD Programming

Normally, the Carrier Controller (Lattice CPLD) is not required to be reprogrammed. However, if the user would like to configure the CPLD with an own bitfile or we recommend an important firmware update, in the following it is described in detail how to do so!

The Lattice LCMXO2-1200HC CPLD device contains two types of memory, SRAM and Flash. While the SRAM contains the active configuration, the Flash memory provides an internal storage space for the configuration data. The SRAM can be configured either via the on-board IEEE 1149.1 compliant FTDI USB-to-JTAG interface or from data stored in the CPLD's on-chip Flash memory. The on-chip Flash can also be programmed via JTAG.

Configuring SRAM or Programming Flash

The JEDEC file created by, e.g., *Lattice Diamond Design Software*, can be simple downloaded (free

download from Lattice website) to the CPLD device via the FTDI USB-to-JTAG interface by the following steps:

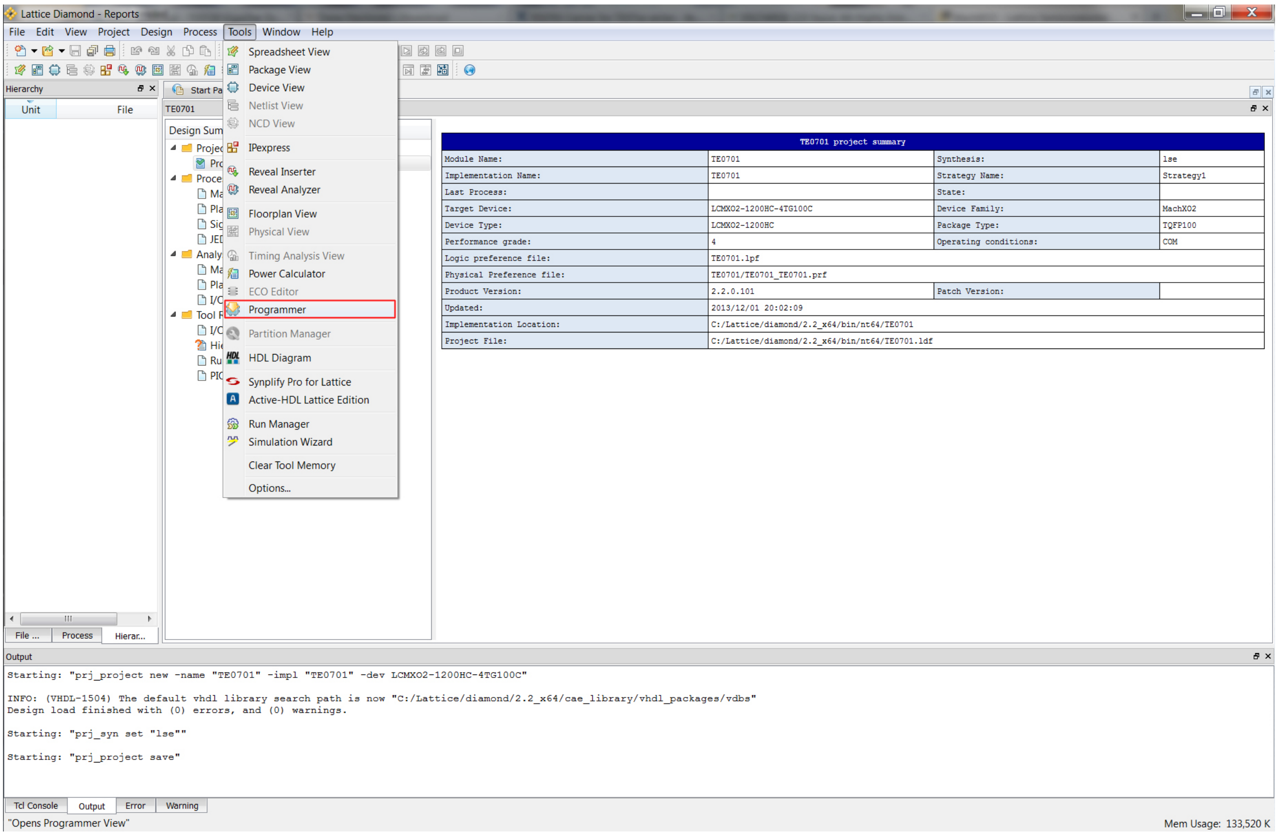
1.) Make sure that JTAG mode is enabled on TE0701 Carrier Board (see section "Jumper Configurations | Configuring CPLD JTAG Mode"):

- TE0701-02 (REV2): Jumper J22 labeled "CPLD JTAG EN" (see Figure 3) has to be REMOVED to enable CPLD JTAG mode.
- TE0701-03 (REV3): DIP switch S3 labeled "ENJTAG" must be moved to OFF position.

2.) Plug-in 12V power supply.

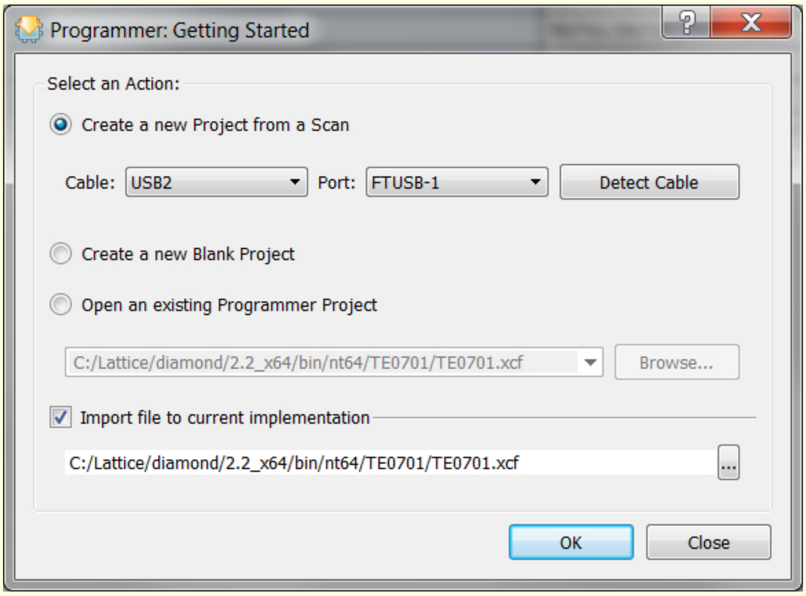
3.) Plug a standard USB A-Male to Mini-B cable into the USB port of the Host PC and into the mini USB connector (see (19) in Figure 1 of TE0701 Carrier Board User Manual) on the TE0701 carrier board.

4.) Open Lattice Diamond and choose Tools -> Programmer:



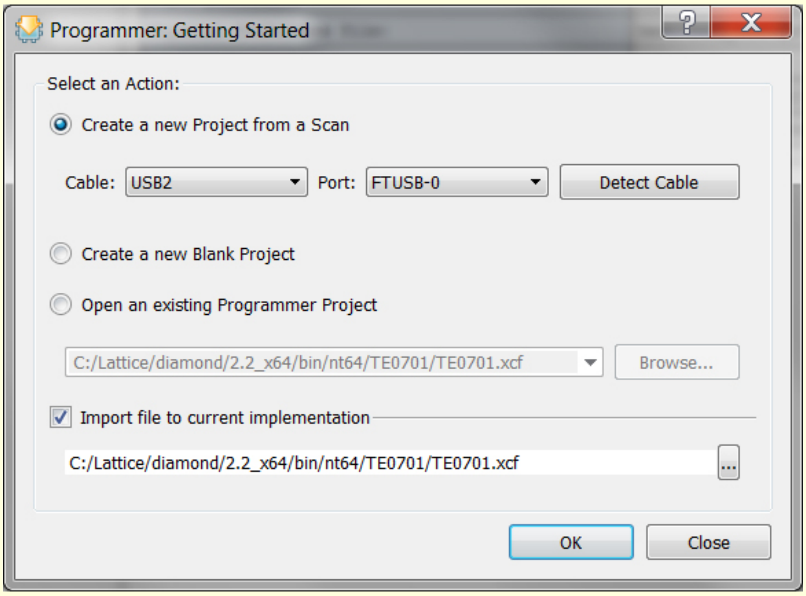
5.) Select in the "Programmer: Getting Started" dialog the following settings:

- TE0701-02 (REV2): FTUSB-1 has to be selected as port, this is Channel B of the on-board FTDI USB-to-JTAG interface:

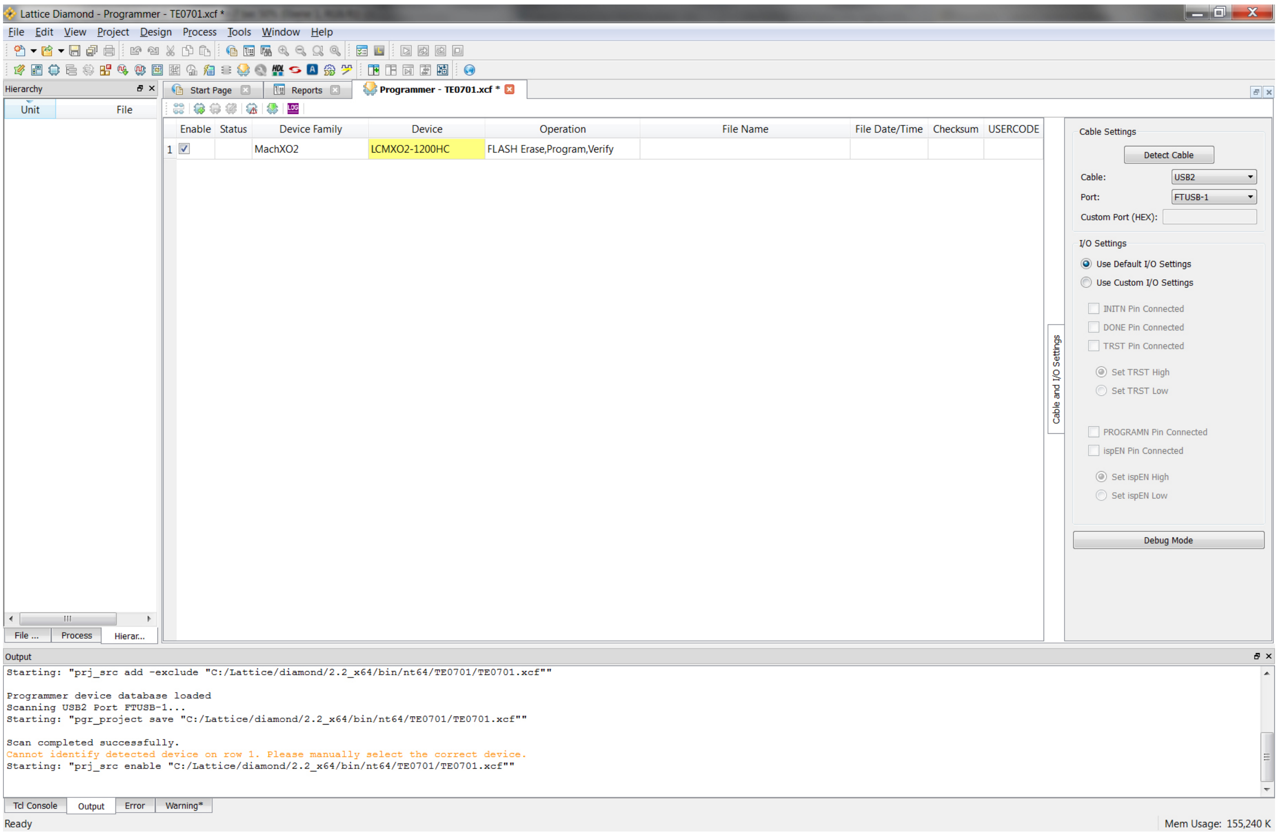


Note: On port 0 (Channel A) of the FTDI USB-to-JTAG interface the JTAG port of the, e.g., Xilinx Zynq FPGA (see *Figure 3*) on the carried module is accessible!

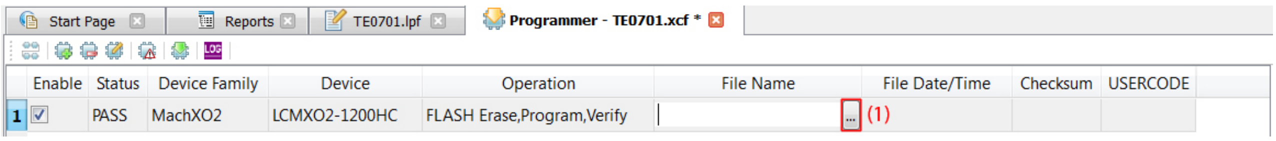
- TE0701-03 (REV3): FTUSB-0 has to be selected as port, this is Channel A of the on-board FTDI USB-to-JTAG interface:



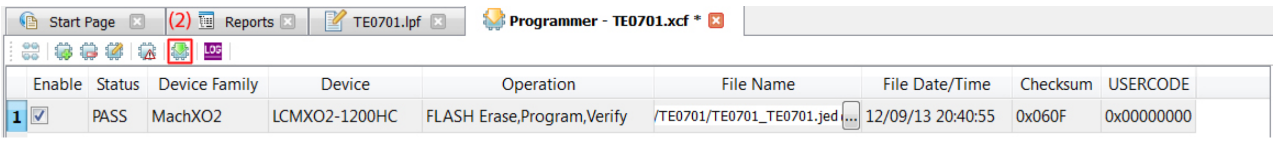
6.) After the scan has been completed successfully, the following GUI should be visible, wherein the LCMXO2-1200HC CPLD device must be selected manually:



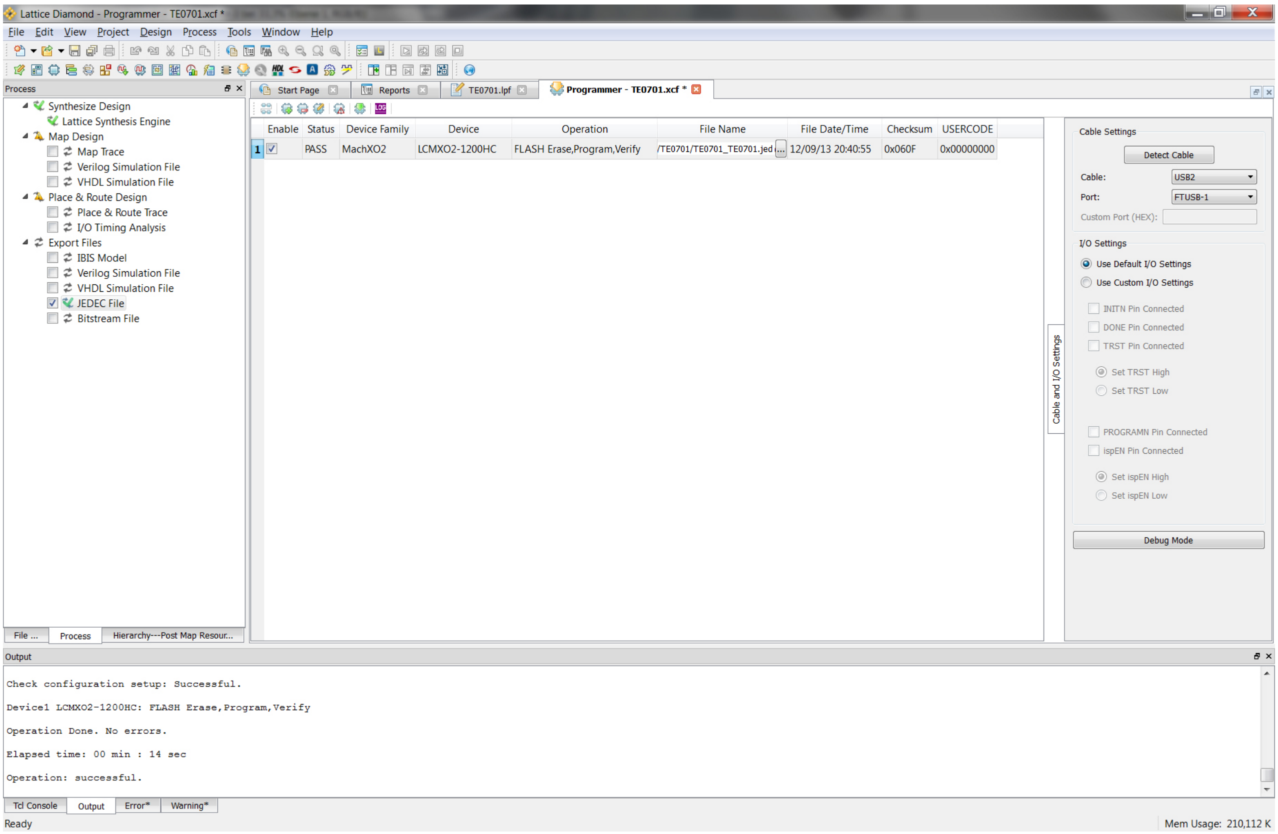
7.) Now the previously generated JEDEC file can be selected (1) ...



8.) ... and the CPLD can be flashed by pushing on the "program" button (2):



9.) Finally, the successful CPLD Flash configuration operation will be confirmed in the output window:



Xilinx Zynq (TE0720 Zynq SoC module) Programming

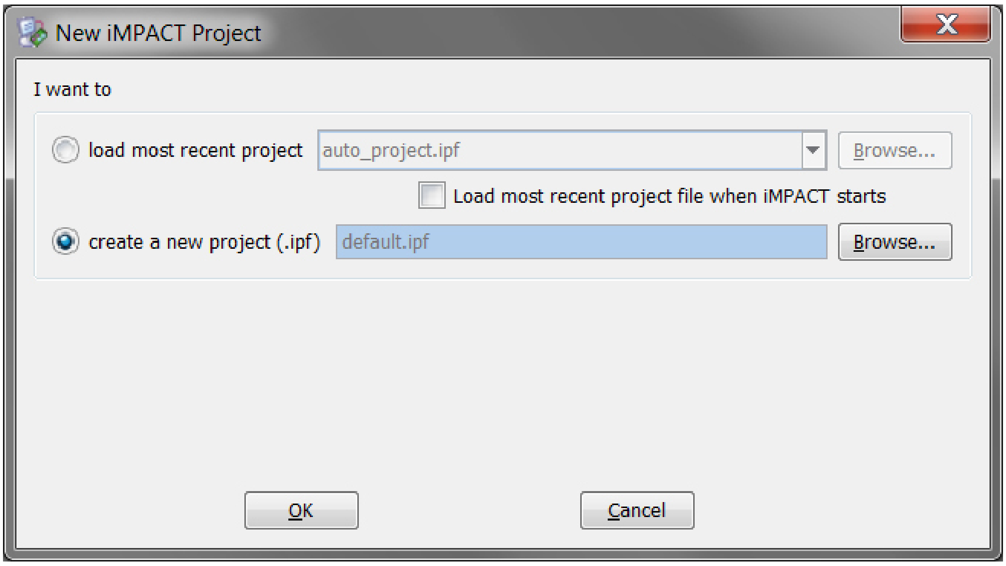
The Xilinx Zynq FPGA on the TE0720 Zynq SoC module can be configured by *Xilinx Design Tools* (particularly, Xilinx iMPACT):

1.) Plug-in 12V power supply.

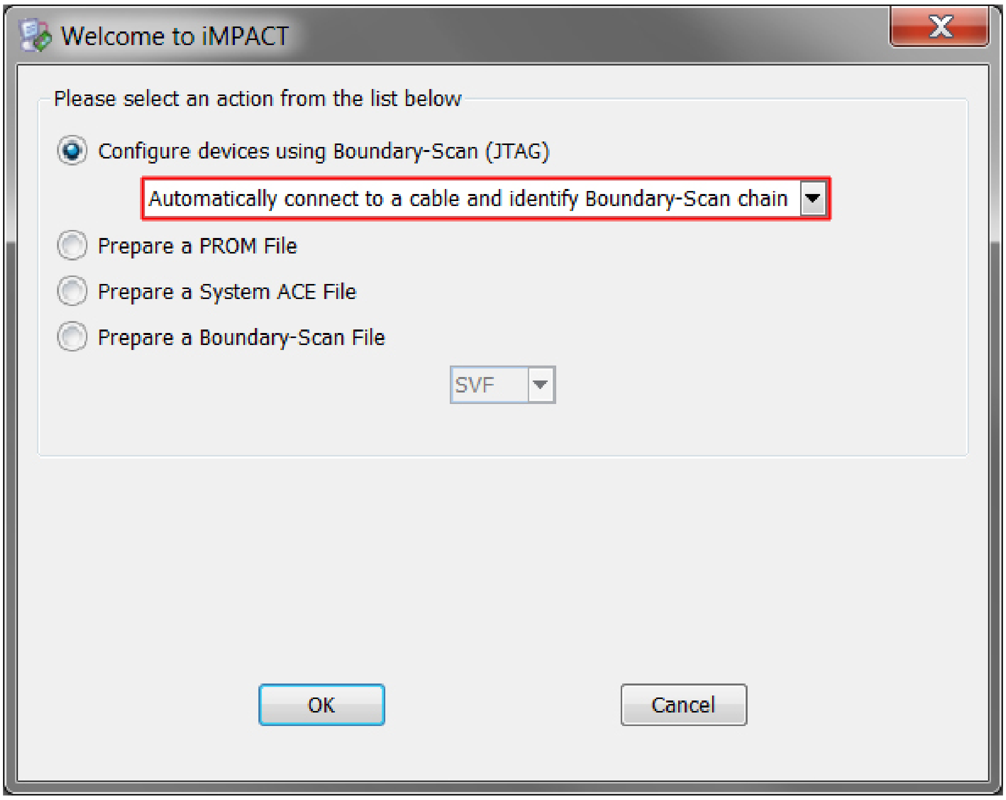
2.) Plug a standard USB A-Male to Mini-B cable into the USB port of the Host PC and into the mini USB connector (see (19) in Figure 1 of TE0701 Carrier Board for TE07xx Series User Manual) on the TE0701 Carrier Board.

3.) Open Xilinx iMPACT (available with free Vivado/ISE WebPack License):

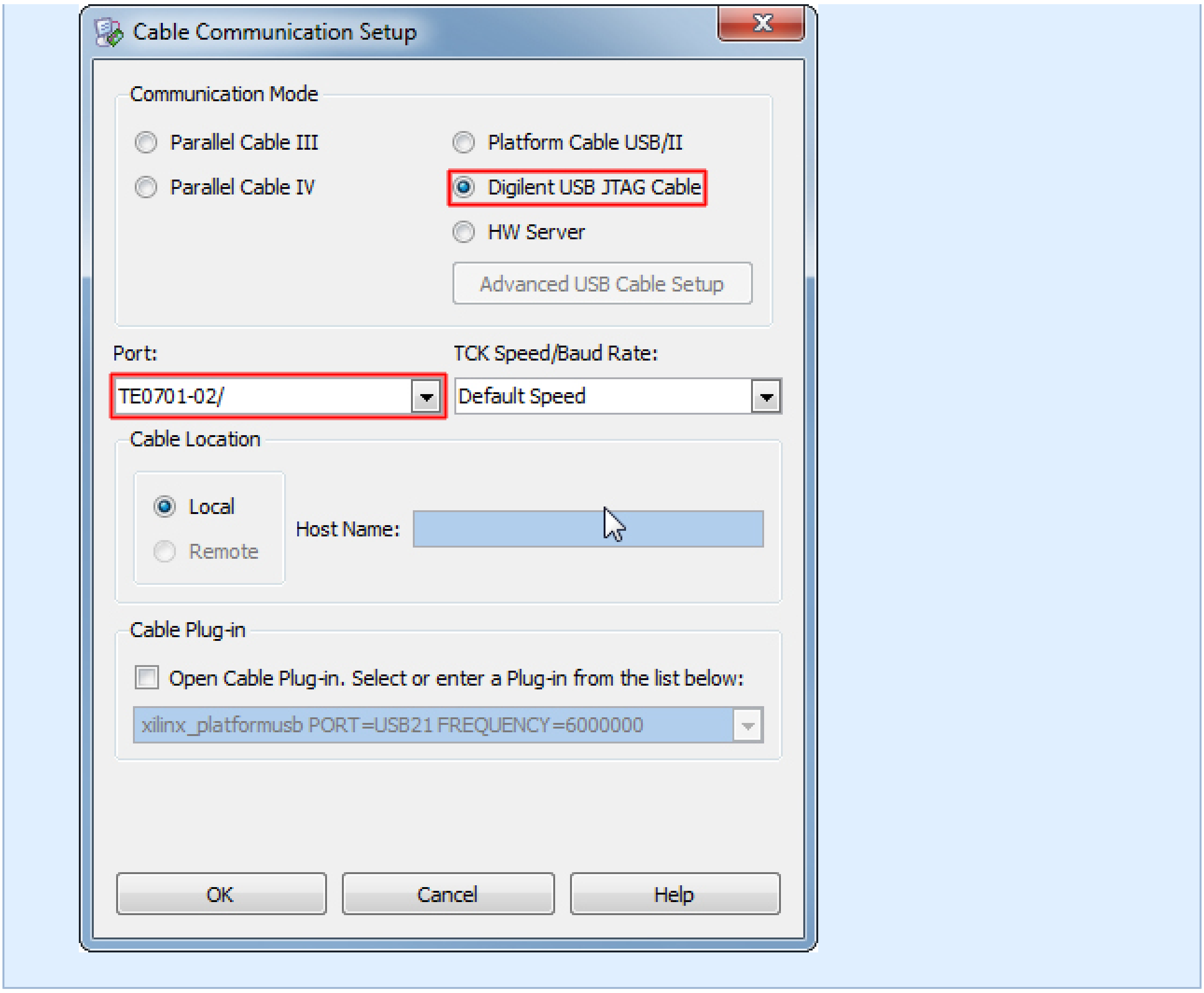
4.) Create a new Xilinx iMPACT project:



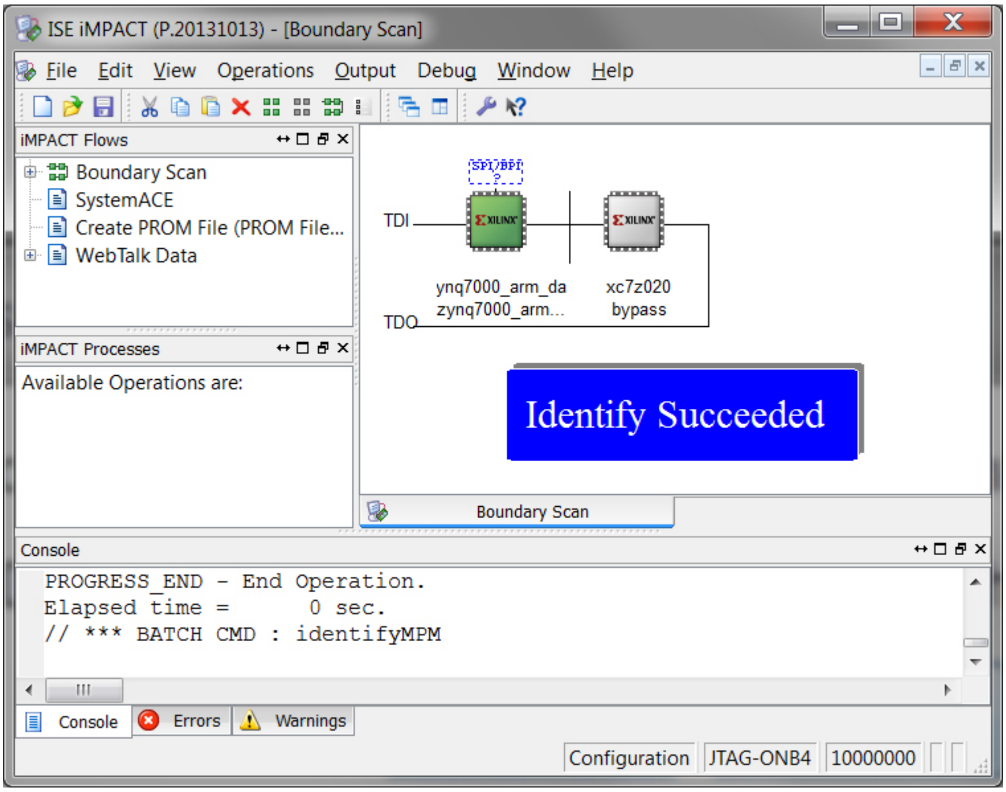
5.) Select to *Configure devices using Boundary-Scan (JTAG)* and choose option "Auto":



When manually choosing "Xilinx Impact 14.7 | Cable Communication Setup" then select "Digilent USB JTAG Cable". **Note**: The port name "TE0701-02/[ID]" is read from FTDI User EEPROM:



6.) After successful identification the following graphical view of the TE0720 JTAG chain will appear, which comprises the *Processing System* (PS) and the *Programmable Logic* (PL) that are now ready to be programmed (please see related Xilinx documentation Zynq-7000 All Programmable SoC Operations in iMPACT for more details):



Most iMPACT Boundary Scan operations performed on a Zynq-7000 AP SoC device are performed on the PL block. For more information about configuring the TE0720 Zynq SoC module, please consult the corresponding Trenz Electronic Wiki documentation.

ARM JTAG Bus

To debug ARM software, the user can route the ARM DAP signals (PJTAG) through the MIO or through the EMIO and to PL SelectIO pins as shown in the following figure (see Xilinx Zynq-7000 AP SoC Technical Reference Manual, UG585 v1.6.1, Figure 27-1 on page 653):

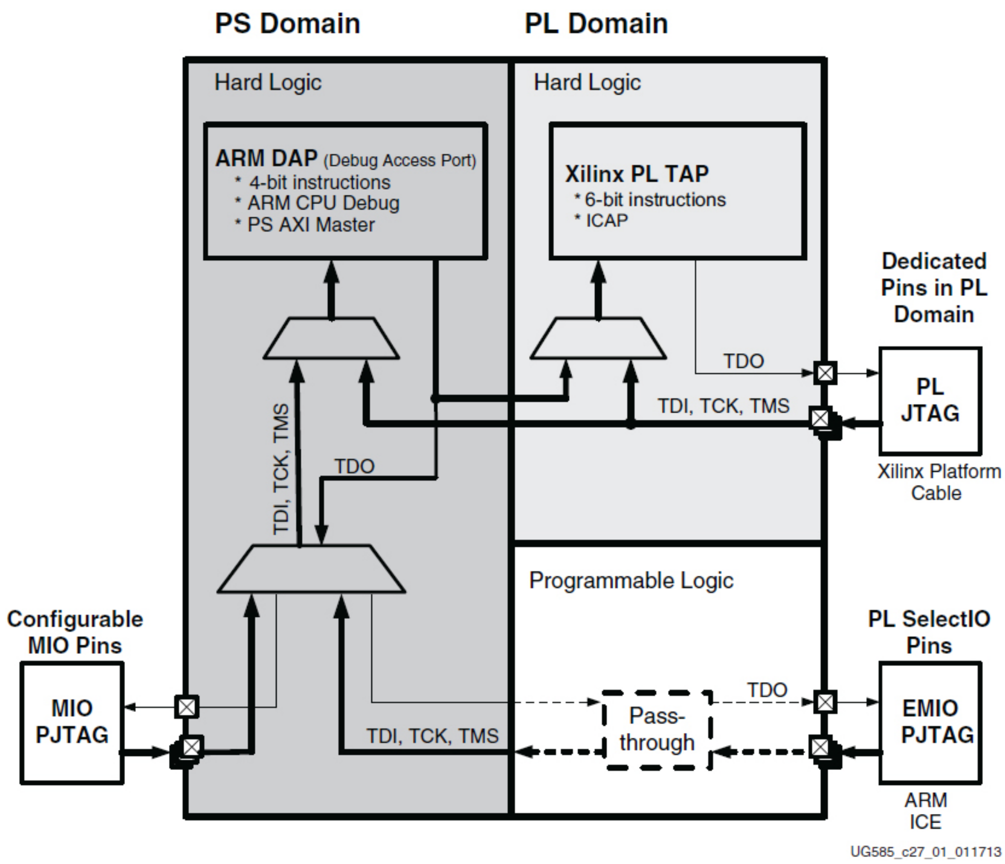


Figure 27-1: **JTAG System Block Diagram**

All dedicated signals of the ARM *Debug Access Port* (DAP) are routed to the Pmod Connector J1 (see (3) in Figure 1 of TE0701 Carrier Board for TE07xx Series User Manual) and (if routed through the Xilinx Zynq EMIO interface) to the ARM JTAG Connector (see (4) in Figure 1 of TE0701 Carrier Board for TE07xx Series User Manual) on the TE0701 Carrier Board.

TE0701 Control and Data Flow with TE0720

Press "<Strg> + <Pos1>" to return back to this overview!

Control and Data Flow on TE0701 and TE0720

The TE0701 Carrier Board comprises several components that can be accessed by the TE0720 Zynq SoC Module. The corresponding control and data flow paths are visualized in the following figure:

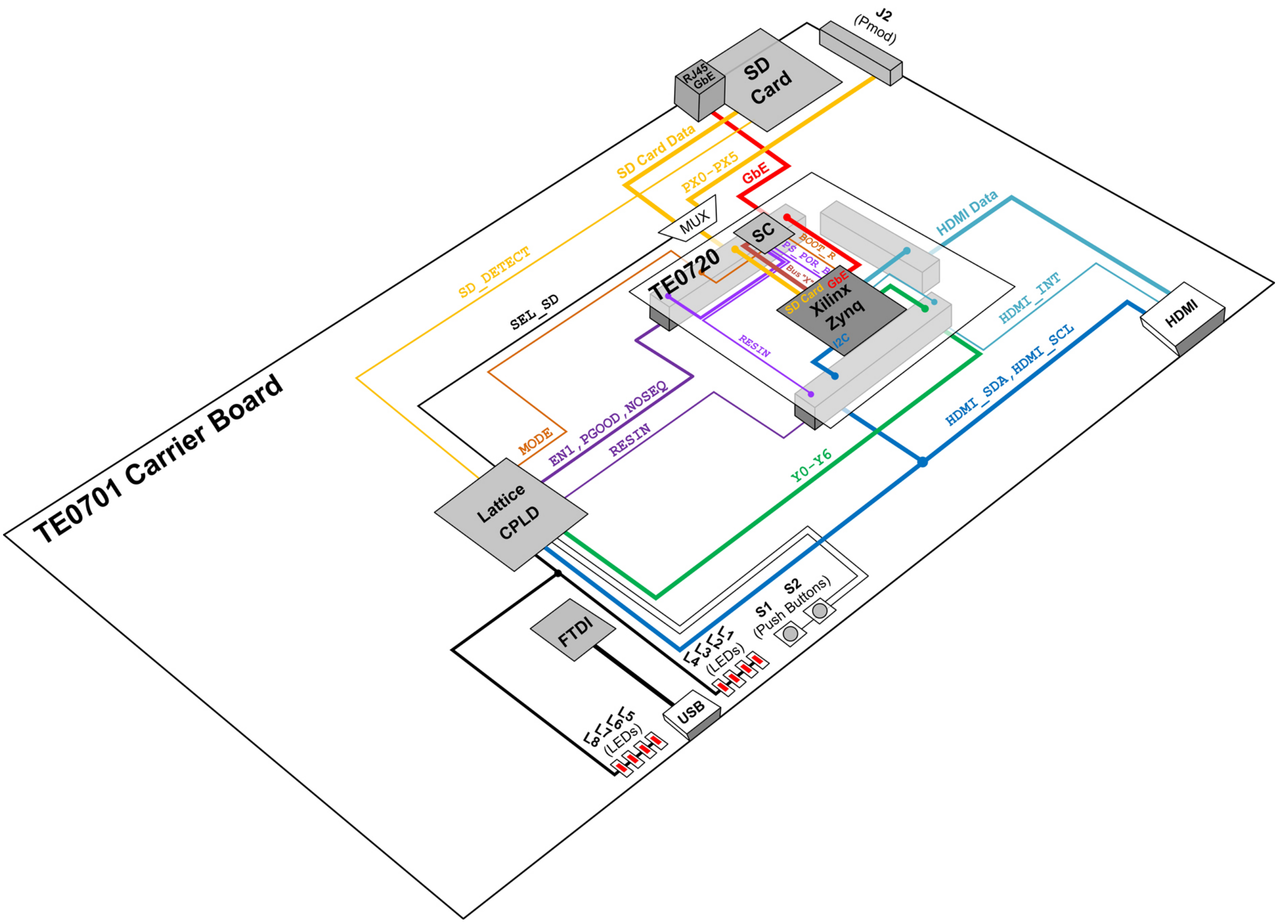


Figure 4a: Control and Data Flow on the TE0701 (REV2) and the TE0720 (REV1) - FMC Connector not shown.

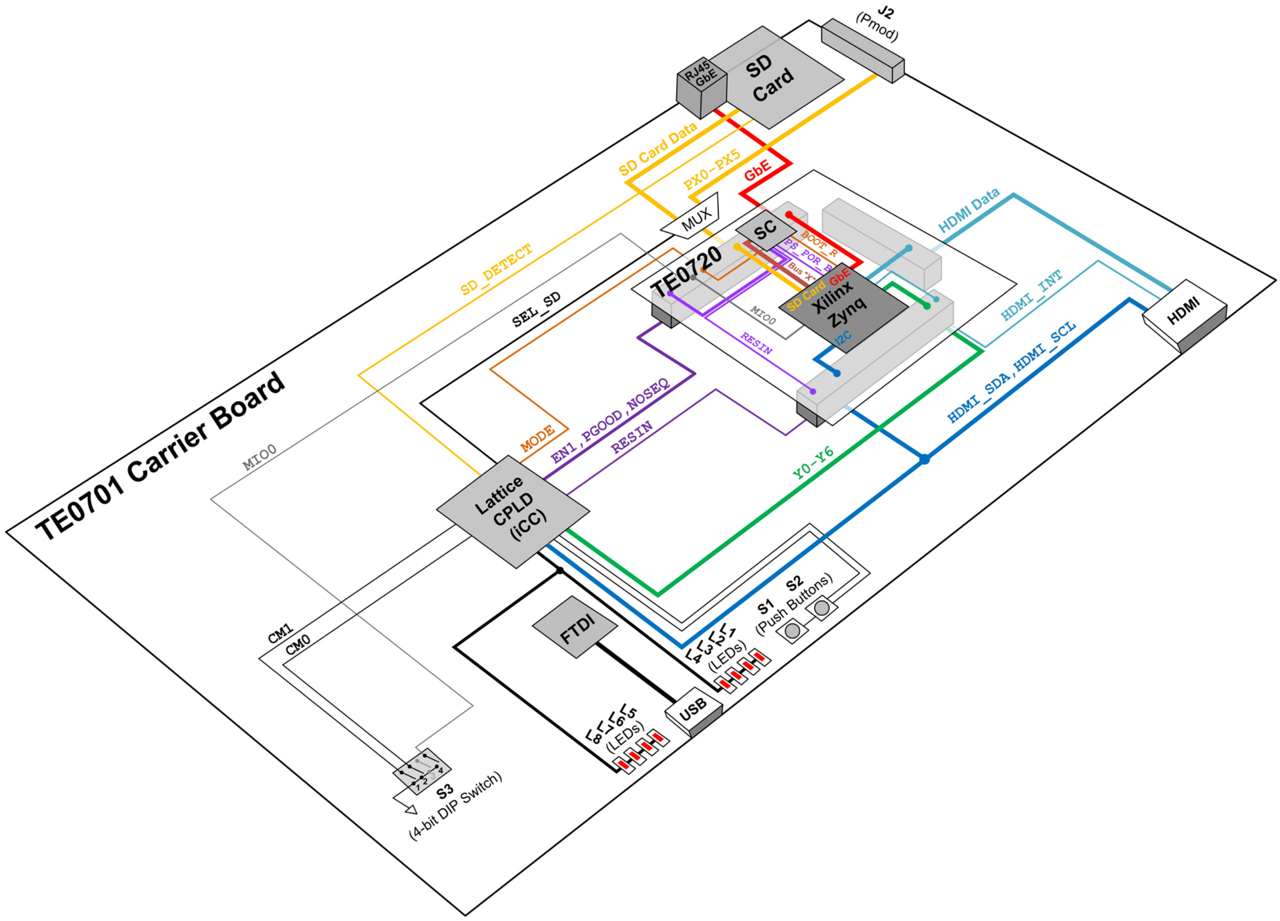


Figure 4b: Control and Data Flow on the TE0701 (REV3) - FMC Connector not shown.

Power On Reset (POR)

On the TE0701 the 5.0V and 3.3V power supply rails are generated by high performance DC-DC Enpirion converters (EN2340QI) from the external 12V supply. While the 3.3V plane supplies several on-board components (e.g., Lattice CPLD and FTDI Dual USB UART/FIFO IC), the 5V plane is mainly provided for power supply of the module to be carried (e.g., TE0720 Zynq SoC module). For the latter, however, special considerations must be taken (see TE0720 Power Supply). Therefore, the on-module *system controller* (SC) must be provided with information about the *power-on-reset* (POR) process, namely, the following control signals EN1, RESIN, and NOSEQ. And the SC provides, in turn, the status signal PGOOD down to the on-board CPLD.

Signal	Description
EN1	This CPLD output active-high signal is a “power on (PON)” signal that is usually HIGH (weak pull-up), except, the user push button S2 is pressed, which forces the related signal to be LOW (ground). EN1 enables (EN1=’1’) and disables (EN1=’0’) the supplies on the carried module, respectively.
RESIN	This signal is controlled by the user push button S1 on the TE0701 and is forwarded directly to the SC, where it is latched together with the EN1 signal as well as the “all power rails OK” signal (1.0V and 1.8V for core; 1.5V and VTT for RAM, and 3.3V). The 3.3V power supply rail can be switched on (EN_3V3=’1’) or off (EN_3V3=’0’) by a load switch (TPS27082L) and is continuously checked by a voltage detector (TPS3805H33). **Note**: The 3.3VIN power supply (from which the 3.3V power plane is sourced) is supplied by the TE0701 Carrier Board and is kept always on!

Signal	Description
	When RESIN (alias user push button S1) is not pushed and simultaneously the EN1 signal is asserted (EN='1') and all power rails are ok, the active-high Zynq *power-on-reset* signal PS_POR_B is asserted.
NOSEQ	This CPLD signal can be used to enable or disable the *power sequencing mode*. If the active-high NOSEQ signal is set to HIGH (NOSEQ='1') then the 1.0V and 1.8V power supplies on the carried module will be forced to be enabled. In *normal mode* (NOSEQ='0') the 3.3V power supply is turned on after the 1.0V and 1.8V supplies have stabilized (see TE0720 Power Supply). The latter is the default mode, i.e., for the NOSEQ pin of the SC the internal pull-down is activated. After booting, the NOSEQ pin can be used as general-purpose I/O pin. For example, the SC (REV 0.02) maps the Ethernet PHY LED0 to NOSEQ by default. However, this mapping can be changed by software after boot.
PGOOD	This active-high signal (with internal pull-up) is a status input to the CPLD about the current status of the power supply rails on the carried module (e.g., TE0720). It is routed to user LED3, which is switched on when the on-module power supply rails are not ok.

For more information on the preceding signals please consult the corresponding Wiki documentation of the TE0720 System Management Controller.

Configuring Boot Mode

The Zynq-7000 generally supports several boot modes that can be selected by five boot mode pins BOOT_MODE[4:0], where BOOT_MODE[4] / MIO[6] enables the PLLs. The other boot mode pins select the boot source in the following way (see Xilinx Zynq-7000 AP SoC Technical Reference Manual, UG585 v1.6.1, Table 6-2 on page 147):

The TE0720 Zynq SoC Module on the TE0701 Carrier Boards supports two different boot modes: QSPI and SD Card booting.

	BOOT_MODE[0] MIO[5]	BOOT_MODE[2] MIO[4]	BOOT_MODE[1] MIO[3]	BOOT_MODE[3] MIO[2]
Cascaded JTAG				0
Independent JTAG				1
JTAG	0	0	0	0
Quad-SPI	**1**	**0**	**0**	
SD Card	**1**	**1**	**0**	

Table 1: Zynq-7000 AP SoC Boot_Mode MIO Pins (Extract)

As it can be seen in Table 1 the only difference between *Quad-SPI* and *SD Card* boot mode is BOOT_MODE[2] / MIO[4]. This is exactly the only signal which is controlled by the MODE output of the on-board CPLD. The BOOT_MODE[0] / MIO[5] and BOOT_MODE[1] / MIO[3] input pins are tightend correspondingly, e.g., on the TE0720 Zynq SoC Module to pull-up (i.e., SPI-DQ3/M3 = PS_MIO5 = 1) and pull-down (i.e., SPI_DQ1/M1 = PS_MIO3 = 0) resistors.

Booting from SD Card

The Quad-SPI boot mode is the default option. However, when a SD card has been inserted into the TE0701 Carrier Board SD Card Connector (see (1) in Figure 1 of TE0701 Carrier Board for TE07xx Series User Manual) the SD Card boot mode is automatically chosen by the on-board CPLD because the active-low SD_DETECT input signal is directly mapped to the MODE output signal (see Figure 4) before booting the Zynq on the carried board (more precisely, the BOOT_MODE signals are sampled 50 PS_CLK ticks after the Low-to-High transition of the PS_POR_B reset pin). Moreover, the LED labeled L4 on the TE0701 is switched on when a SD card is inserted.

Choosing between Cascaded and Independent JTAG

Two different JTAG modes can be selected by the dedicated on-module PJTAG_R signal: *Cascaded* JTAG (BOOT_MODE[3] / MIO[2] = PJTAG_R = 0) and *Independent* JTAG (BOOT_MODE[3] / MIO[2] = PJTAG_R = 1). In Cascaded JTAG mode (i.e., single chain mode) one JTAG cable (connected to the FTDI USB-to-JTAG interface; see (19) in Figure 1 of TE0701 Carrier Board for TE07xx Series User Manual) can be used to have access both to Zynq PS and PL features concurrently. To debug ARM software and the PL design simultaneously with separate cables, the independent JTAG mode must be chosen (**Note**: Please see section "JTAG Programming Guide - ARM JTAG Bus" for more details).

User Push Buttons (PBs) and LEDs

On the TE0701 (REV2 and REV3) Carrier Board two push buttons (S1 and S2) and eight LEDs (L1 to L8) are available to the user. The default PB mapping is as follows:

Name	Default Mapping:
S1	If S1 is pushed, the active-low RESet IN (RESIN) signal will be asserted. **Note**: This reset can also be forced by the FTDI USB-to-JTAG interface.
S2	If S2 is pushed, the active-high Power ON (PON) signal (that is internally pulled-up) will be deasserted, which can be considered as a "RESTART" button to switch *off* (push button) and *on* (release button) all on-module power supplies (except 3.3VIN). **Note**: The capability to be enabled the first time will become active shortly after *Power on Reset* (POR). The active-high PON signal is directly mapped to the active-high EN1 signal which is routed to the SC (e.g., on the TE0720) and directly used (after deglitching) as a mandatory active-high enable signal to the power FET switch (3.3VIN -> 3.3V) as well as the three Enpirion DC-DC converters (VIN -> 1.0V, 1.5V, 1.8V).

All LEDs are red colored and connected to the on-board Lattice CPLD. The default LED mapping is summarized in the following (**Note**: LED5 to LED8 have not been assigned yet):

Name	Default Mapping:
LED1 (L1)	NOSEQ: This active-high signal switches the LED on when the *power sequencing mode* is disabled.
LED2 (L2)	NOT (POK_FMC): The active-high signal POK_FMC is turned on when the FMC power supply FMC_VADJ is present. **Note**: FMC_VADJ may be enabled when FMC is present (FMC_PRSNT=1) and disabled (FMC_PRSNT=0) otherwise!
LED3 (L3)	NOT (PGOOD): The active-high signal PGOOD switches on the LED when the (on-module) power supply is not ok.
LED4 (L4)	NOT (SD_DETECT): SD_DETECT is active-low, i.e., the LED is turned on when a SD card has been inserted.

Table 2: On-board LEDs on TE0701 (REV2 and REV3)

> LED5 (L5) to LED8 (L8) are operating only when the corresponding power supply VIOTB (i.e., bank 1 of the on-board CPLD) is switched on. This can be accomplished on the one hand by connecting the FMC power supply FMC_VADJ to VIOTB (J21: 1,**2-3**), which is the default option, or on the other hand by connecting either 2.5V (J17: 1,**2-3**) or 3.3V (J17: **1-2**,3) to VIOTB (J21: **1-2**,3). Please note that for the first default option, the FMC power supply must be manually switched on by the, e.g., Zynq FPGA on the TE0720 (for more details on configuring the FMC power supply, please refer to Carrier Boards for TE0720 | Configuring FMC Power Supply Voltage on TE0701 via I2C).

4-bit DIP Switch (TE0701-03 only)

Additionally, on the TE0701-03 (REV 3) Carrier Board a 4-bit DIP switch (S3; see (21) in Figure 1 of TE0701 Carrier Board for TE07xx Series User Manual) is available. The default S3 mapping is as follows:

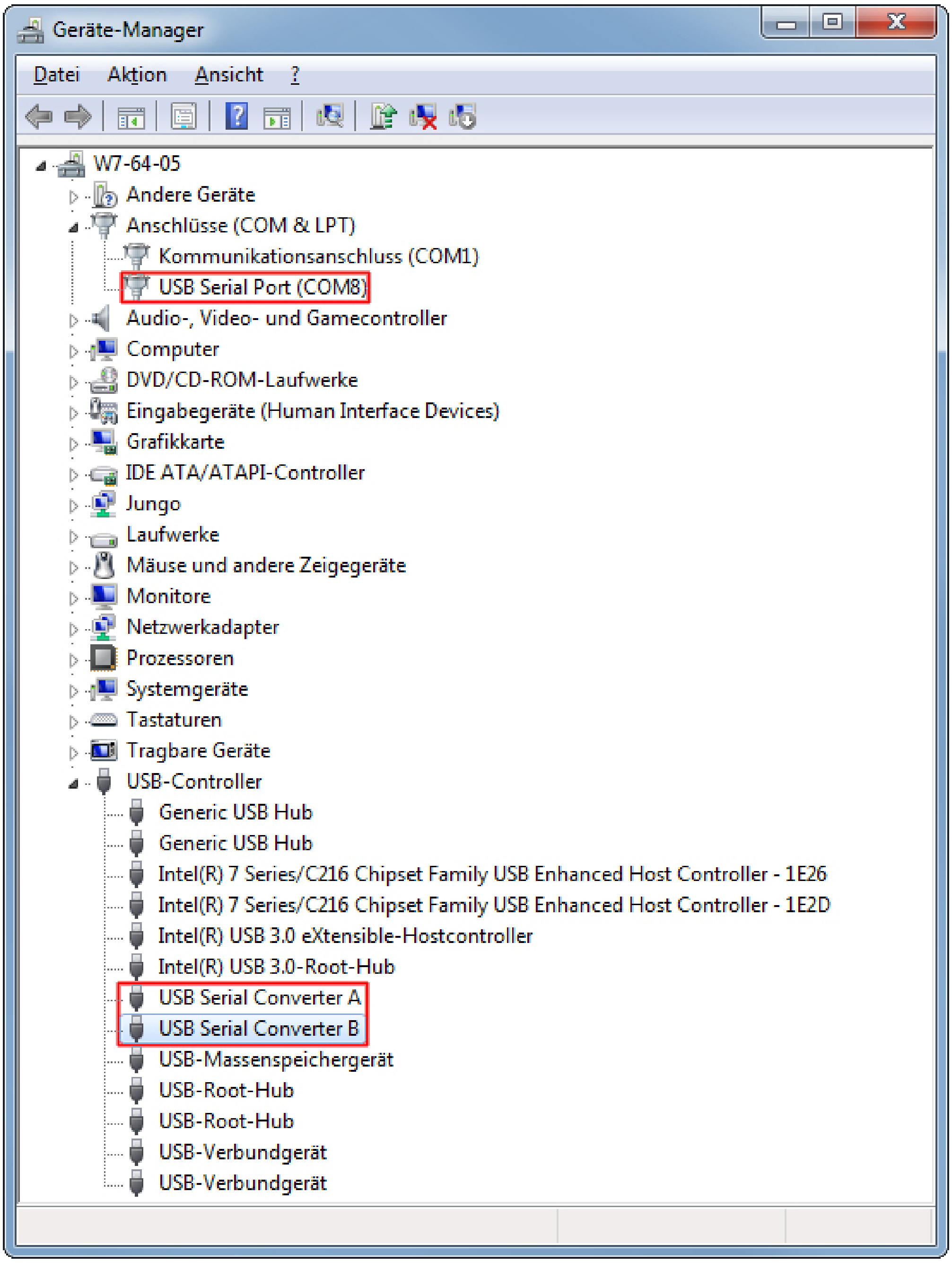
Name	Default Mapping:
S3-1	CM1: Mode pin 1 (routed to Carrier Controller)
S3-2	CM0: Mode pin 0 (routed to Carrier Controller)
S3-3	JTAGEN: Set to ON for normal operation. Must be moved to OFF position to enable JTAG programming mode (see TE0701 Carrier Board User Manual | Lattice CPLD Programming for more details)
S3-4	MIO0: Readable signal by Carrier Controller and TE07xx Module

All Connecting FTDI USB-to-UART/FIFO Interface

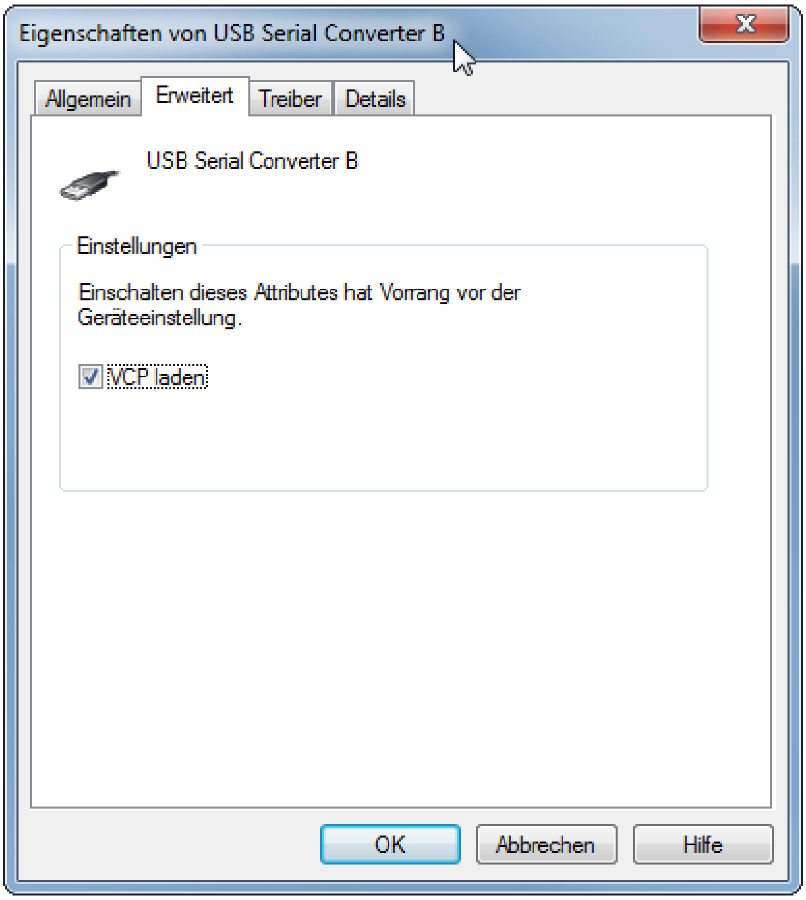
On TE0701-02 (REV2) and TE0701-03 (REV3) the UART of the FPGA (e.g., Xilinx Zynq) on the carried module can be connected to the host PC via channel B of the on-board FTDI - Dual USB UART/FIFO IC (FTDI FT2232H), which is routed to the mini USB connector (see (19) in Figure 1 of TE0701 Carrier Board for TE07xx Series User Manual).

> There is by default no USB communication when connecting the **micro USB connector** to the host PC (see (15) in Figure 1 of TE0701 Carrier Board for TE07xx Series User Manual).

On a Windows 7 host PC the FTDI FT2232H USB-to-UART/JTAG interface should be shown in the device manager as two serial converters (channel A and channel B) and a one virtual USB COM port...



... if "VCP Loading" for "USB Serial Converter B" is enabled (**Note**: Converter A VCP Loading should be disabled):

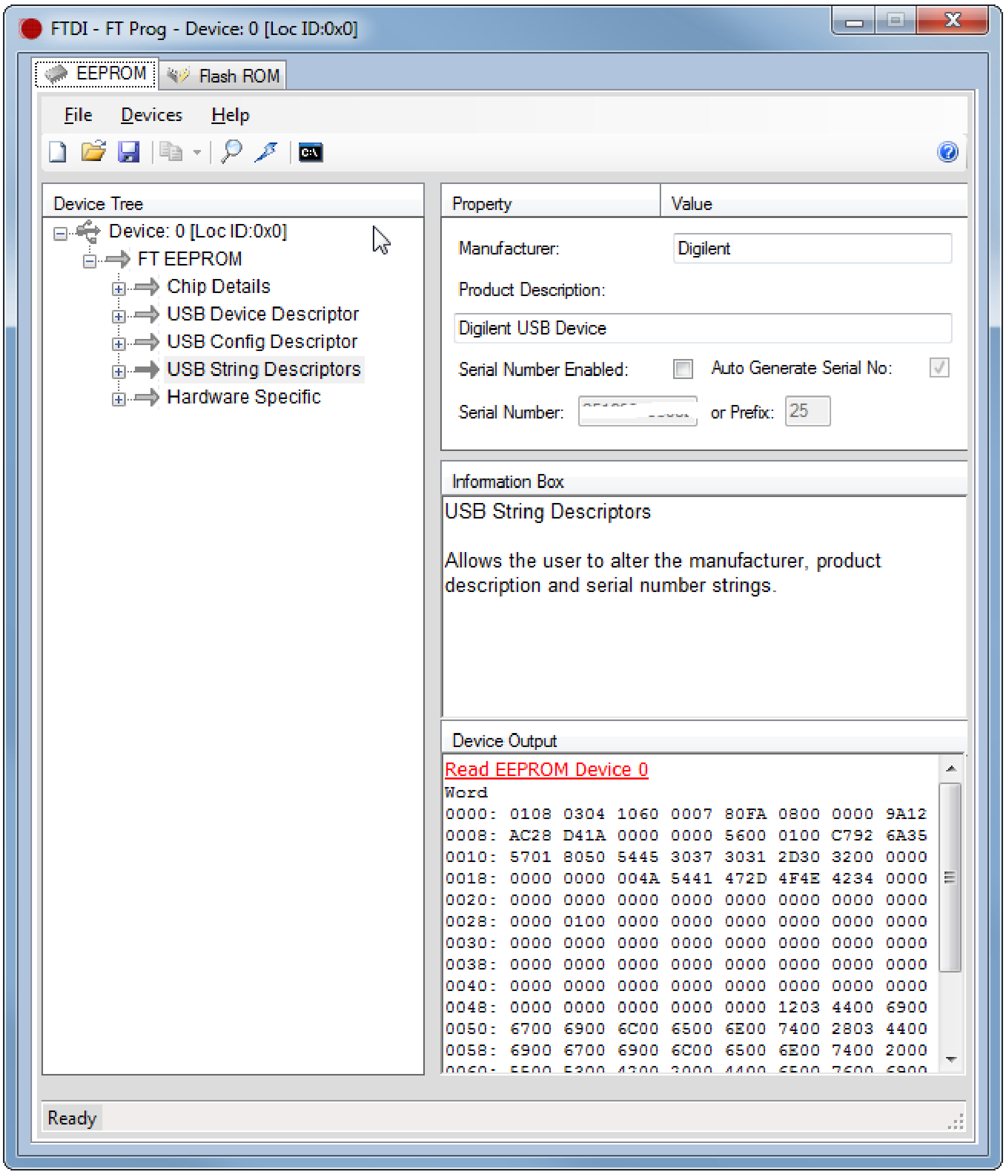


IMPORTANT NOTE on Using FTDI Tools

The FTDI Tool "FT Prog" can only be used to display the FTDI device name and to check if it is correct.

When using FTDI USB Tools DO NOT WRITE the on-board FTDI EEPROM on TE0701! All FTDI tools overwrite the user EEPROM area on each EEPROM write without any warning. Erased user EEPROM will disable Xilinx tools support for the on-board USB JTAG!

This is how on-board USB JTAG should look in "FT Prog":



It is not possible to use FTDI FT Prog to restore EEPROM! Should the EEPROM be overwritten, special tools are required.

Intelligent Carrier Controller

Starting from rev 1.0 the Carrier Controller includes an Softcore Processor that can configure the hardware on TE0701 and implement many additional functions.

Function Multiplexing

TODO!!!

Interactive mode

In interactive mode ICC accepts simple commands over serial port (UART settings 8N1, 115200 baud). As default (when all ICC nonvolatile memory is erased) TE0701 on-board USB IC (FTDI FT2232H) channel B is used for communications. If FTDI Channel B is selected as communication channel for ICC then it is disconnected from other sources.

Commands

Erase all

This command will perform a bulk erase of user flash memory of the ICC. All settings, and user programs stored will be lost, and factory default settings for the ICC will apply.

Identify/Info

This command will display Identification and other Information about the ICC and the Carrier Board

Command code: "i"

Example

```
BAS:IC>i ID:012BA043 FMC:0 SD:1W:1
```

ICC returns its own JTAG IDCODE (identifies the IC as Lattice XO2-1200HC), FMC Card Detect (0 - no card detected), SD Card Detect: Card detected, not write protected (note: if no card is inserted Write Protect swith would read 1, eg not locked).

FMC Interface

FMC VADJ Control

To enable FMV_VADJ on TE0701 bit 7 of I²C register 0x22 should be set.

Requirements

In FPGA PS project some Zynq I²C controller should be enabled and connected to EMIO. For example we use I²C controller 0.

In FPGA PL project this controller signals should be connected to pins W20 (signal HDMI_SCL on TE0701) and W21 (signal HDMI_SDA on TE0701).

Enabling FMV VADJ from U-Boot

In u-boot configuration enable selected I²C bus. (Controller 0 in our example)

```
#ifdef CONFIG_ZYNQ_I2C
# define CONFIG_CMD_I2C
# define CONFIG_HARD_I2C 1
# define CONFIG_SYS_I2C_SPEED 100000
# define CONFIG_SYS_I2C_SLAVE 1
# define CONFIG_ZYNQ_I2C_CTLR_0
#endif
```

In u-boot command line interface check that device with address 0x22 is visible.

```
zynq-uboot> i2c probe
Valid chip addresses: 22 38 39 3C 3E 3F
```

and set bit 7 by write command

```
zynq-uboot> i2c mw 0x22 0x80 1
```

Enabling FMV VADJ from Linux

In linux device tree selected I²C controller should be enabled and configured.

```
i2c0: i2c@e0004000 {
compatible = "xlnx,ps7-i2c-1.00.a";
reg = <0xE0004000 0x1000>;
interrupts = <0 25 4>;
interrupt-parent = <&gic>;
```



```
bus-id = <0>;
input-clk = <100000000>;
i2c-clk = <400000>;
};
```

In linux command line interface check that device with address 0x22 is visible.

```
zynq> i2cdetect -y -r 0
     0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f
00:          -- -- -- -- -- -- -- -- -- -- -- -- --
10: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
20: -- -- 22 -- -- -- -- -- -- -- -- -- -- -- -- --
30: -- -- -- -- -- -- -- -- 38 39 -- -- 3c -- 3e 3f
40: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
50: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
60: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
70: -- -- -- -- -- -- -- --
```

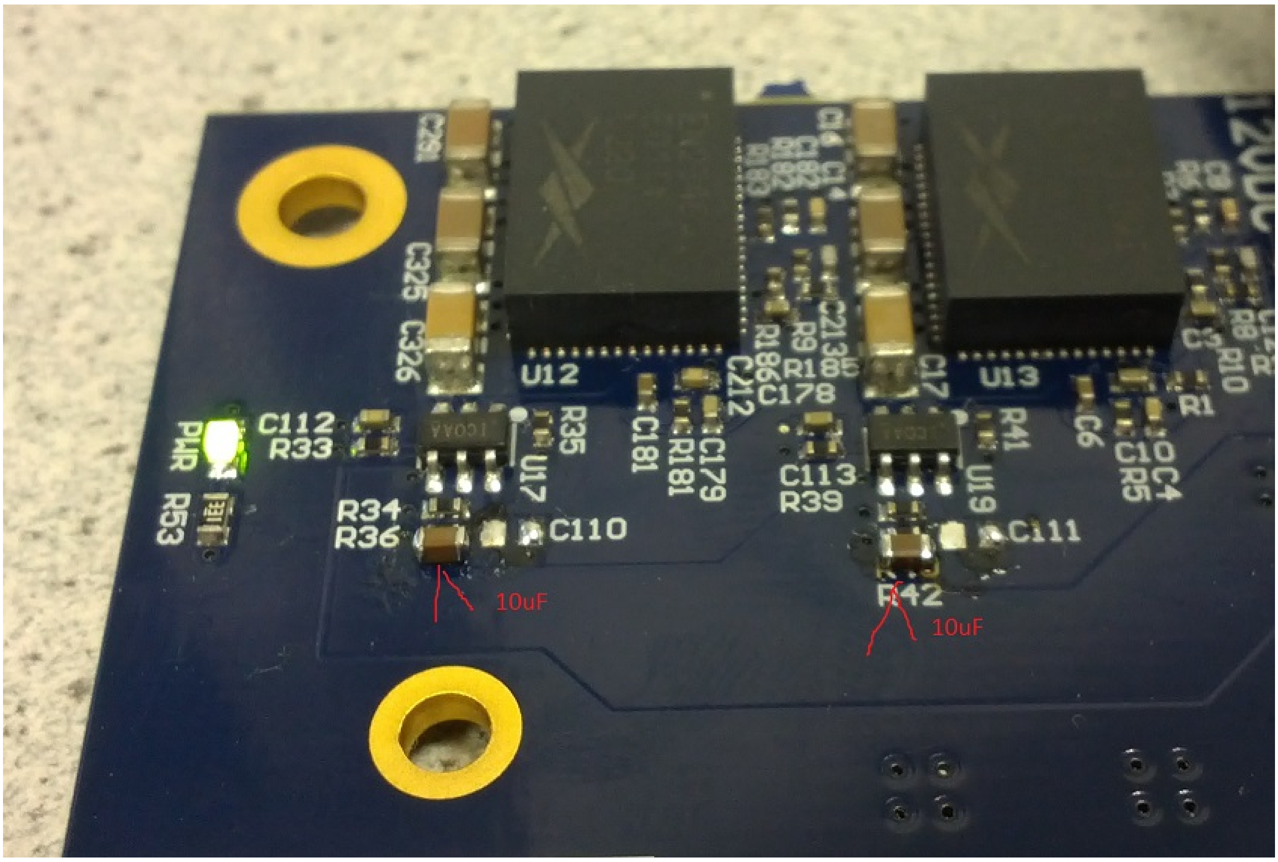
and set bit 7 by write command

```
zynq> i2cset -y 0 0x22 0x80
```

TE0701 (REV2) Known Issues

First batch of TE0701 shipped did not have proper inrush current/slew rate limiting circuitry required by the Enpirion newest datasheet rev C. This can cause damage to the 3.3V and/or 5V DCDC converters if power is applied by pushing in power plug. This will cause the 12V input at Enpirion VIN terminals to rise in about 40uS what is 50x times more than allowed in datasheet.

This slew rate absolute maximum rating violation MAY cause damage to the Enpirion DC-DC converters on TE0701. This has never happened in the lab or in factory testing where we use different power supplies and stress the boards. However, failures have been reported at customer sites. If your TE0701 does not boot up properly and both red and green led stay lit, then this may be caused by a damaged 5V regulator. Moving the jumper on J16 to different position usually allows the board to be used with 3.3V supplied to module VIN.



TE0701 PCB with the slew rate patch applied, 2 capacitors 10uF each are added in parallel to existing resistors (R36 and R42) on PCB, also remove C110 and C111.

This fix will not repair the DCDC converter should it be already damaged.

Ethernet RJ45

TE0701 has a RJ45 MAGJACK with two LED's.

PHY LED's are not connected directly to the module B2B connectors as the 4x5 modules have no dedicated PHY LED pins assigned. PHY LED's are connected on the TE0701 to the carrier controller, that can route those LED's to some module I/O Pins. In that case the Module has to map the PHY LEDs to corresponding pins.

With initial Carrier Controller design, one RJ45 LED (the right one) is connected to module NOSEQ pin that functions as PHY LED output on TE0720 with default settings. The other LED is connected to I2C GPIO Extender and can be controlled from TE0720 if desired. This LED will not have PHY LED function on TE0701 with System Controller version 0.x

Pmod Slots

J5 and J6 Pmod signal routing is done as differential pairs for pins 1-2, 3-4, 7-8, 9-10

PMOD J5

Pin	Module/B2B	BSP Name	TE0720	TE0710	TE0712	TE0741
1	JM2.22	TE0701_J5_GPIO[0]	W17			
2	JM2.24	TE0701_J5_GPIO[1]	W18			
3	JM2.21	TE0701_J5_GPIO[2]	Y19			
4	JM2.23	TE0701_J5_GPIO[3]	AA19			
7	JM2.26	TE0701_J5_GPIO[4]	W16			
8	JM2.28	TE0701_J5_GPIO[5]	Y16			
9	JM2.25	TE0701_J5_GPIO[6]	Y18			
10	JM2.27	TE0701_J5_GPIO[7]	AA18			

PMOD J6

Pin	Module/B2B	BSP Name	TE0720	TE0710	TE0712	TE0741
1	JM2.	TE0701_J6_GPIO[0]				
2	JM2.	TE0701_J6_GPIO[1]				
3	JM2.	TE0701_J6_GPIO[2]				
4	JM2.	TE0701_J6_GPIO[3]				
7	JM2.	TE0701_J6_GPIO[4]				
8	JM2.	TE0701_J6_GPIO[5]				
9	JM2.	TE0701_J6_GPIO[6]				
10	JM2.	TE0701_J6_GPIO[7]				

TE0703 Carrier Board User Manual

Overview: TE0703 Carrier Board

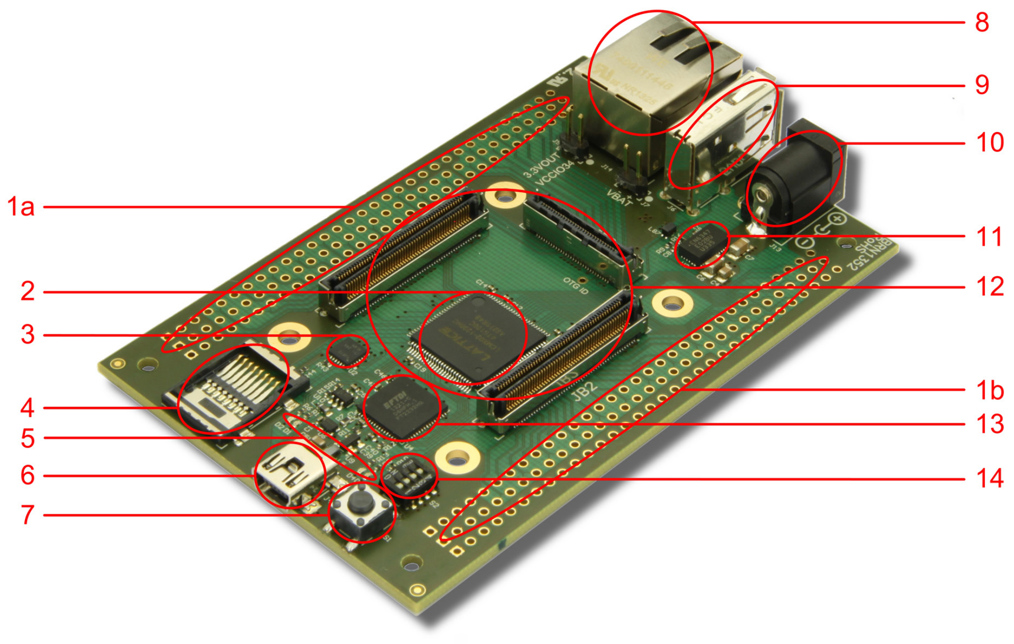


Figure 1: TE0703 (REV 01).

Features

1. VG96 Connector (Mounting Holes and Solder Pads)
2. Carrier Controller CPLD (Lattice LCMXO2-1200HC): 1,200 Macrocell CPLD with Block RAM, Flash and PLL;
   4 User LEDs and 1 User Pushbutton mappable to different functions (see TE0703 Carrier Board User Manual | Lattice CPLD Programming)
3. SDIO Port Expander with Voltage-Level Translation (Texas Instruments TXS02612)
4. Micro SD Card Connector - Zynq SDIO0 Bootable SD port
5. User LEDs (function mapping depends on TE0703 CPLD Carrier Controller, see TE0703 Carrier Board User Manual | User LEDs)
6. Mini USB Connector (USB JTAG and UART Interface, see TE0703 Carrier Board User Manual | JTAG Programming Guide)
7. User Push Button ("RESET", see TE0703 Carrier Board User Manual | Push-Button)
8. RJ45 GbE Connector
9. USB Host Connector
10. Barrel jack for 5V* Power Supply
11. 4A High-Efficiency Power SoC DC-DC Step-Down Converter with Integrated Inductor (Enpirion EN6347) for 3.3V Power Supply

12. Trenz 4x5 Module Socket (3x Samtec LSHM Series Connectors)
13. USB JTAG and UART Interface (FTDI FT2232H), compatible with Xilinx Tools (also with many other tools):
    Channel A can toggle Zynq SoC Module (PS) Reset, Channel B can be used as USB UART (TE0703 CPLD can reroute RXD/TXD signals)
14. User DIP Switch

*) **Note**: Contrary to our TE0701 Carrier Board, the TE0703 is powered by a 5V power supply!

Document Change History

date	revision	authors	description
2014-02-12	0.1	Antti Lukats, Sven-Ole Voigt	Work in progress
	All	Antti Lukats, Sven-Ole Voigt	

TE0703 Jumper Configurations

Press "<Strg> + <Pos1>" to return back to this overview!

Jumper Configurations

On the TE0703 carrier board (REV1) different hardware/software configurations can be chosen by the following one jumper J5 and a 4-bit DIP switch:

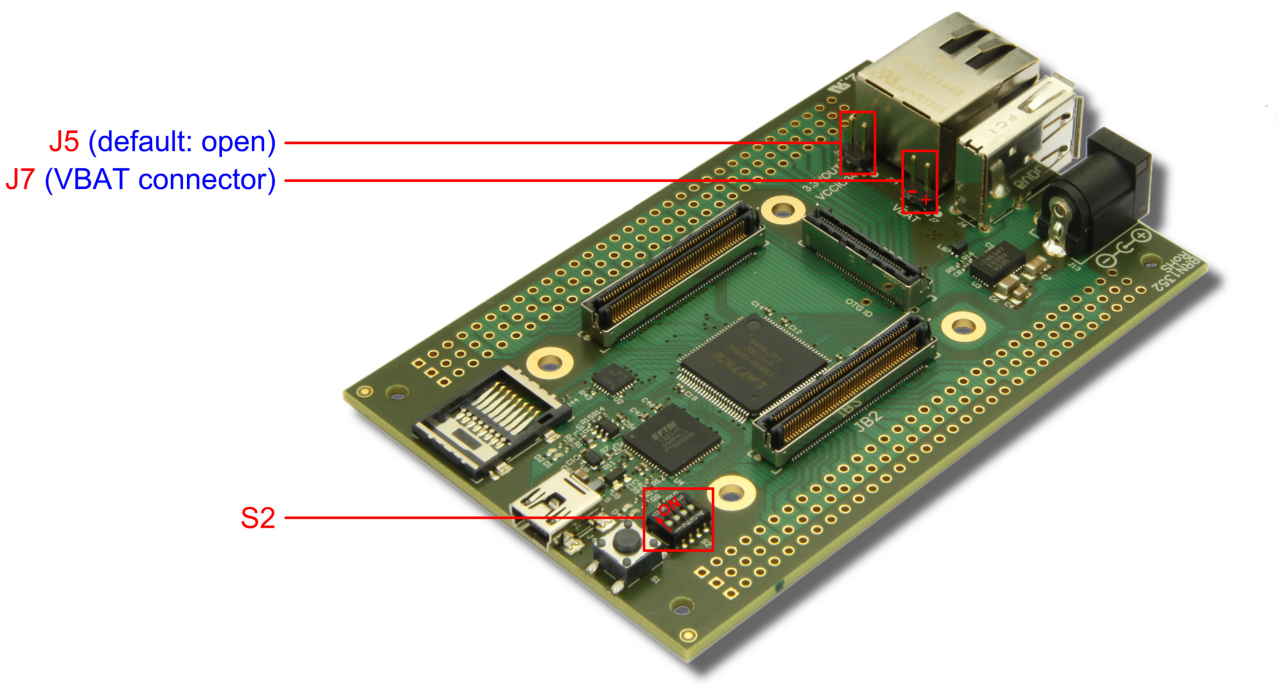


Figure 2: TE0703 (REV1) Jumper Configurations.

Intelligent Carried Controller (iCC) Update Mode

Carrier Controller JTAG port is enabled by setting switch 3 on DIP switch S2 on TE0703-01 (REV1) to "OFF" position. This setting is only useful when updating Carrier Controller firmware!

Switch 3 on DIP switch S2 must be moved to "ON" position for normal operation! Otherwise the JTAG on the module would not be accessible at all.

Configuring B34 Bank Supply of the TE0720 Zynq SoC Module

J5 Jumper can be used to power TE0720 bank 34 from TE0720 3.3V output rail. If J5 is installed TE0720 will boot also in the case bank 34 supply is not delivered from the VG96 /Pin headers. If TE0720 bank supply of 3.3V is required it is recommended to insert the jumper. Optionally, 3.3V or any other valid IO voltage can be supplied from the TE0703 pins.

Backup Battery Supply (VBAT connector)

J7 provides two pins (+/-) to supply battery backup voltage to TE0720. If not required leave open.

Ensure to connect the supply battery to jumper J7 with correct polarity!

TE0703 JTAG Programming Guide

> Press "<Strg> + <Pos1>" to return back to this overview!

JTAG Programming Guide

The Lattice CPLD on TE0703 carrier board as well as the Xilinx Zynq FPGA on the TE0720-GigaZee board can be programmed via JTAG. In the following figures the dedicated JTAG chains are illustrated:

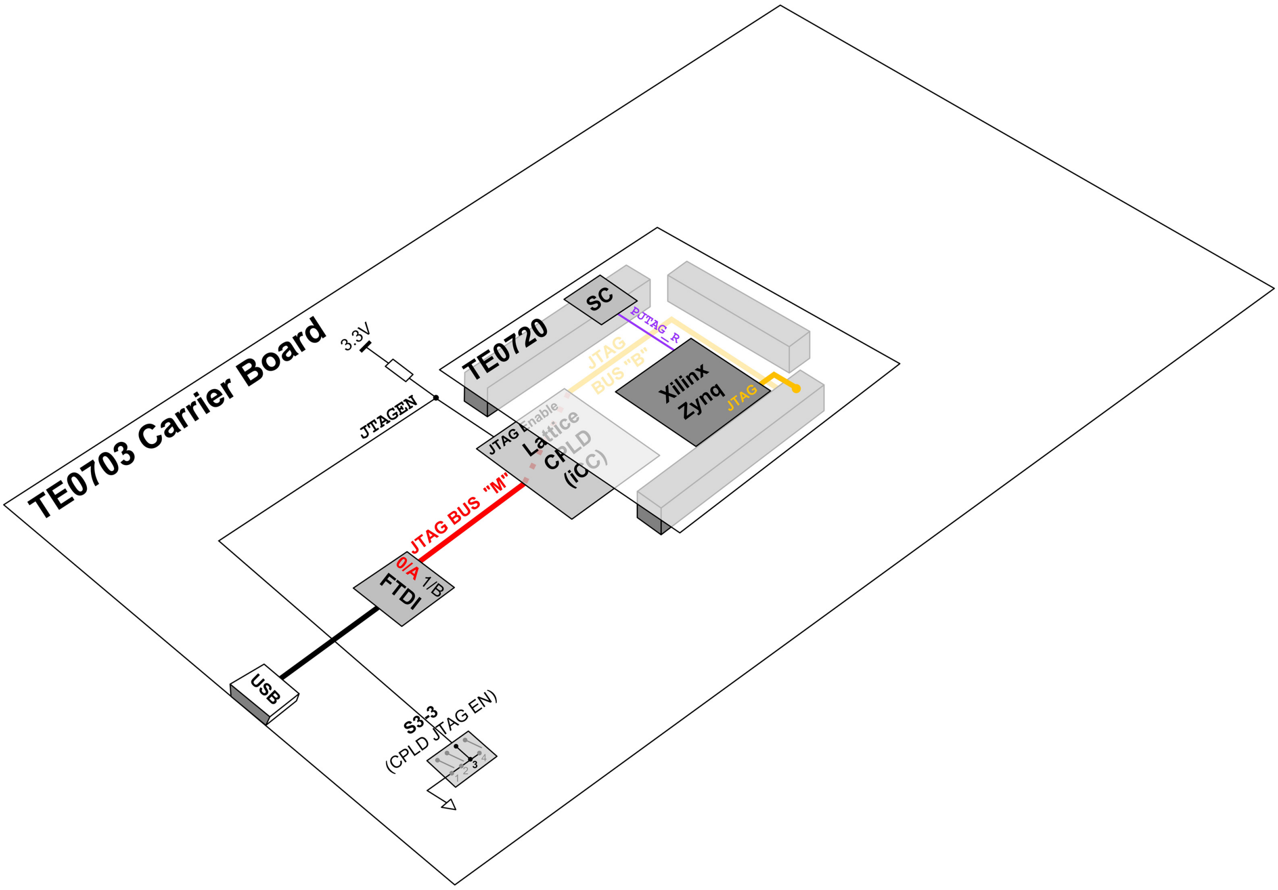


Figure 3: TE0703 and TE0720 (REV1) JTAG Chains.

Lattice CPLD Programming

> Normally, the Carrier Controller (Lattice CPLD) is not required to be reprogrammed. However, if the user would like to configure the CPLD with an own bitfile or we recommend an important firmware update, it is similarly described for the TE0701 (REV3) in TE0701 Carrier Board User Manual | Lattice CPLD Programming!

Xilinx Zynq (TE0720 Zynq SoC module) Programming

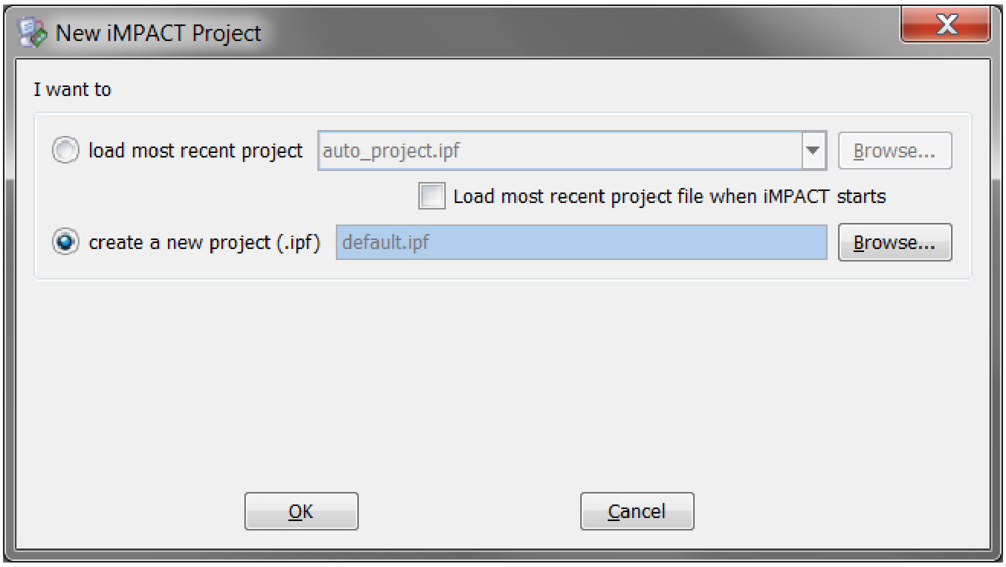
The Xilinx Zynq FPGA on the TE0720 Zynq SoC module can be configured by *Xilinx Design Tools* (particularly, Xilinx iMPACT):

1.) Plug-in 5V power supply.

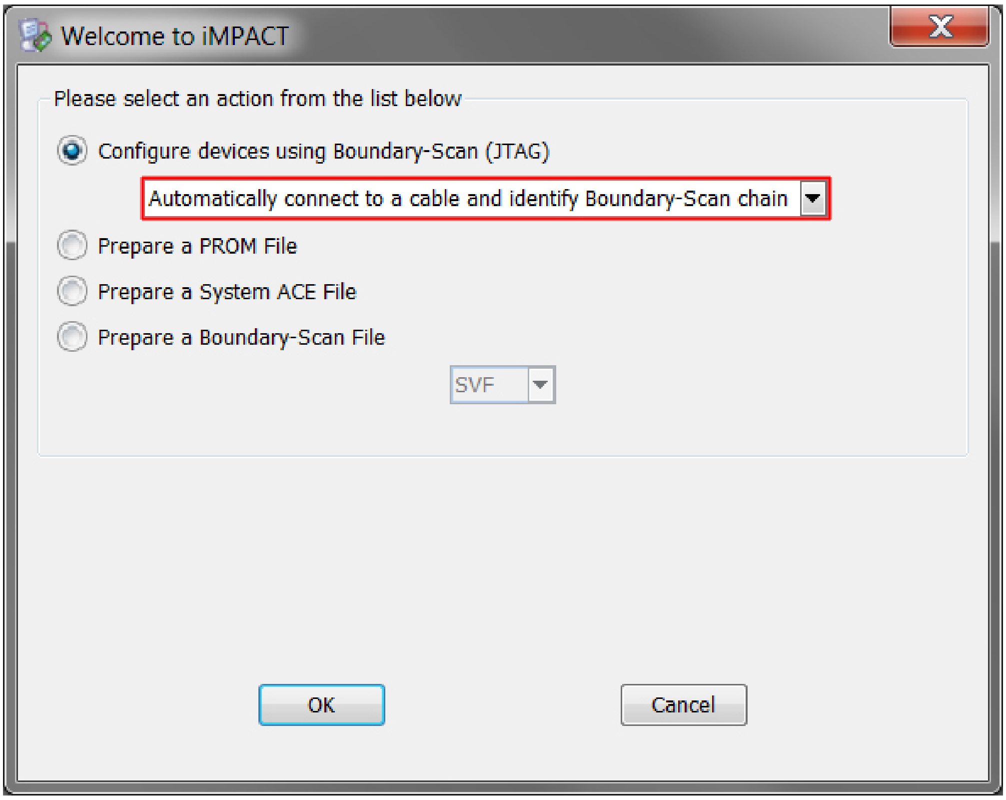
2.) Plug a standard USB A-Male to Mini-B cable into the USB port of the Host PC and into the mini USB connector (see (6) in Figure 1 of TE0703 Carrier Board for TE07xx Series User Manual) on the TE0703 Carrier Board.

3.) Open Xilinx iMPACT (available with free Vivado/ISE WebPack License):

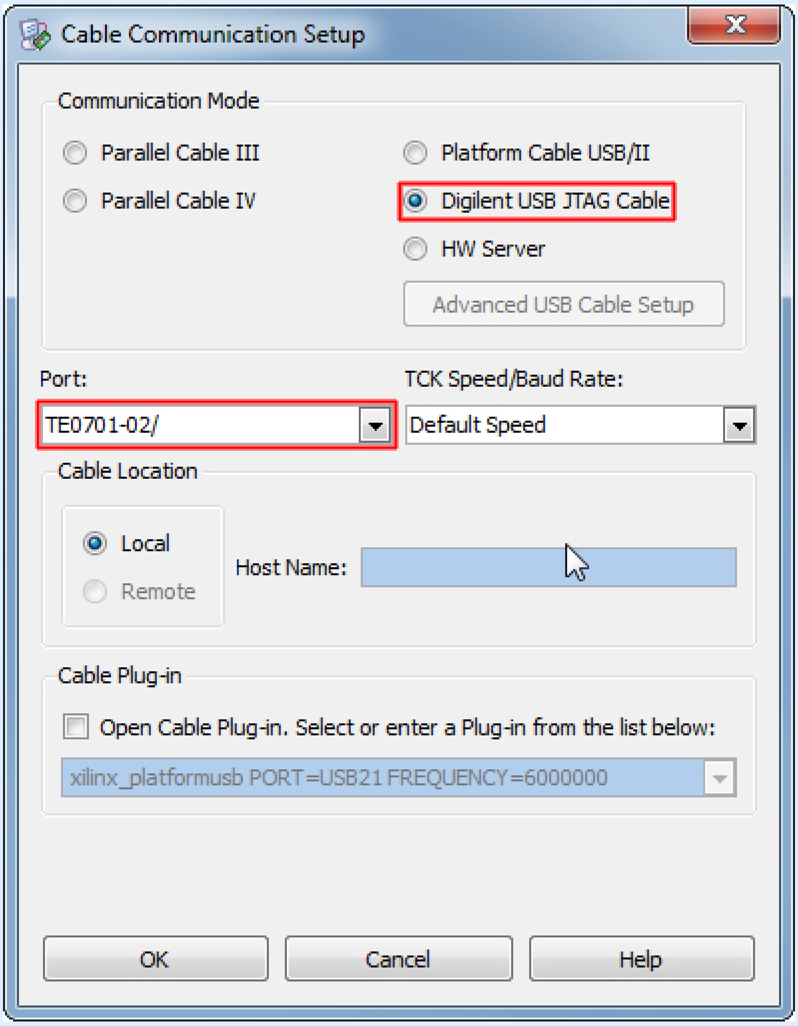
4.) Create a new Xilinx iMPACT project:



5.) Select to *Configure devices using Boundary-Scan (JTAG)* and choose option "Auto":

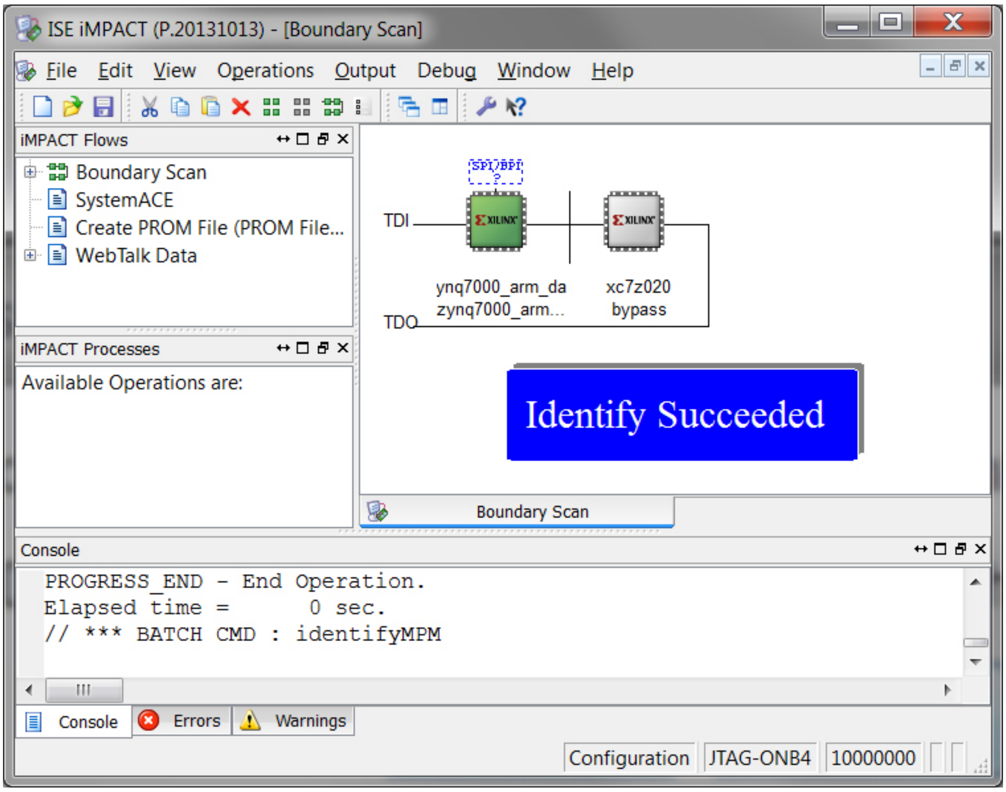

Welcome to iMPACT
Please select an action from the list below
Configure devices using Boundary-Scan (JTAG)
Automatically connect to a cable and identify Boundary-Scan chain
Prepare a PROM File
Prepare a System ACE File
Prepare a Boundary-Scan File
SVF
OK
Cancel

When manually choosing "Xilinx Impact 14.7 | Cable Communication Setup" then select "Digilent USB JTAG Cable". **Note**: The port name "TE0703-01/[ID]" is read from FTDI User EEPROM:



TODO!!!

6.) After successful identification the following graphical view of the TE0720 JTAG chain will appear, which comprises the *Processing System* (PS) and the *Programmable Logic* (PL) that are now ready to be programmed (please see related Xilinx documentation Zynq-7000 All Programmable SoC Operations in iMPACT for more details):



Most iMPACT Boundary Scan operations performed on a Zynq-7000 AP SoC device are performed on the PL block. For more information about configuring the TE0720 Zynq SoC module, please consult the corresponding Trenz Electronic Wiki documentation.

TE0703 Control and Data Flow with TE0720

> Press "<Strg> + <Pos1>" to return back to this overview!

Control and Data Flow on TE0703 and TE0720

The TE0703 Carrier Board comprises several components that can be accessed by the TE0720 Zynq SoC Module. The corresponding control and data flow paths are visualized in the following figure:

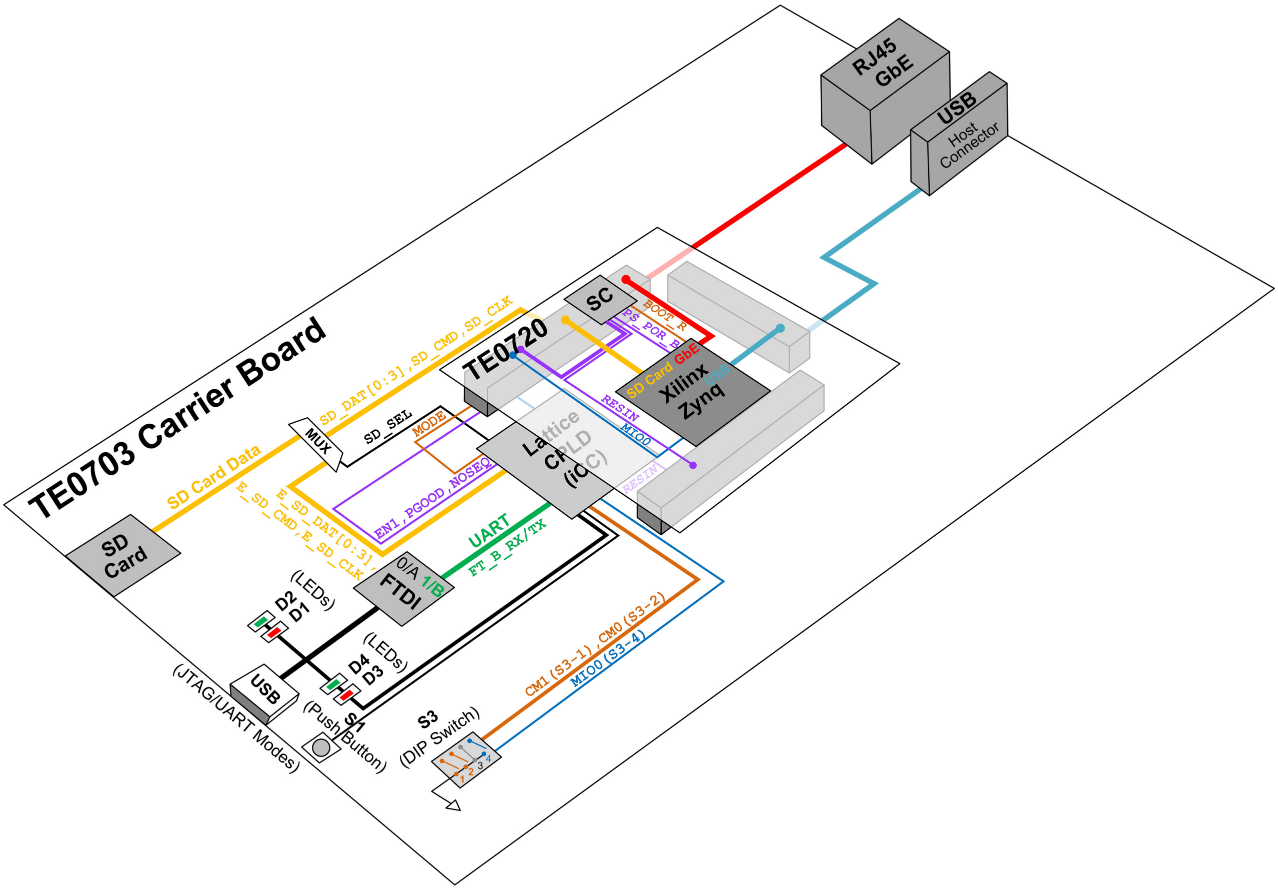


Figure 4: Control and Data Flow on the TE0703 and the TE0720 (REV1)

Intelligent Carrier Controller (iCC)

Features

- Lattice XO2-1200 TQFP100
- 8Bit Softcore Processor
- 2KByte bootrom
- 4KByte Instruction RAM, directly writeable as RAM (write only!)
- 1Kbyte Data RAM
- 8KByte Flash memory (for code and parameter storage)

User LEDs

There are 4 LED's total on TE0703. Two LEDS D1 and D2 are connected to the Carrier Controller, their function depends on the Firmware. LED's D3 and D4 are connected to the 4x5 Module B2B Connector pins, and are directly controlled by the module.

Push-Button

Push-button S1 is connected to "intelligent Carrier Controller (iCC)" and can be used as module reset button. Other usage possible, actual function depend on the code loaded into iCC.

DIP Switch

4 bit DIP switch has following functions:

- enable/disable update of the "intelligent Carrier Controller"
- MIO0 (readable signal by iCC and Module)
- 2 "Mode" bits

LEDs

Module FPGA User LED's

Two LED's (those closer to mini-USB Connector) are connected to the 4x5 B2B Connector pins. Those LEDs can be controlled by FPGA Module.

LED	Net Name	Color	B2B/Module	BSP Name	TE0720	TE0710	TE0712	TE0741
D3	FLED1	Red	JM2.89	TE0703_LEDS[0]	U7	U8	J16	U21
D4	FLED2	Green	JM2.100	TE0703_LEDS[1]	R7	K6	M17	Y20

The bank where LED's are is not powered when TE0703 is used in standalone mode. VCCIO for this bank must be supplied back to the TE0703 connectors. TE0703 header Pin J2.B1 must have some valid I/O voltage or the LED's will not be lit.

System LED's

Two LED's close to the microSD Card are controlled by the Control CPLD, their function depends on the CPLD Version and operational mode.

I2C

Net		B2B/Module	TE0720	TE0710-01	TE0712	TE0741
SCL		JM1.95		M13		
SDA		JM1.93		L18		

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WEEE (Waste Electrical and Electronic Equipment)

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment.

Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

